UROPEAN EDITION

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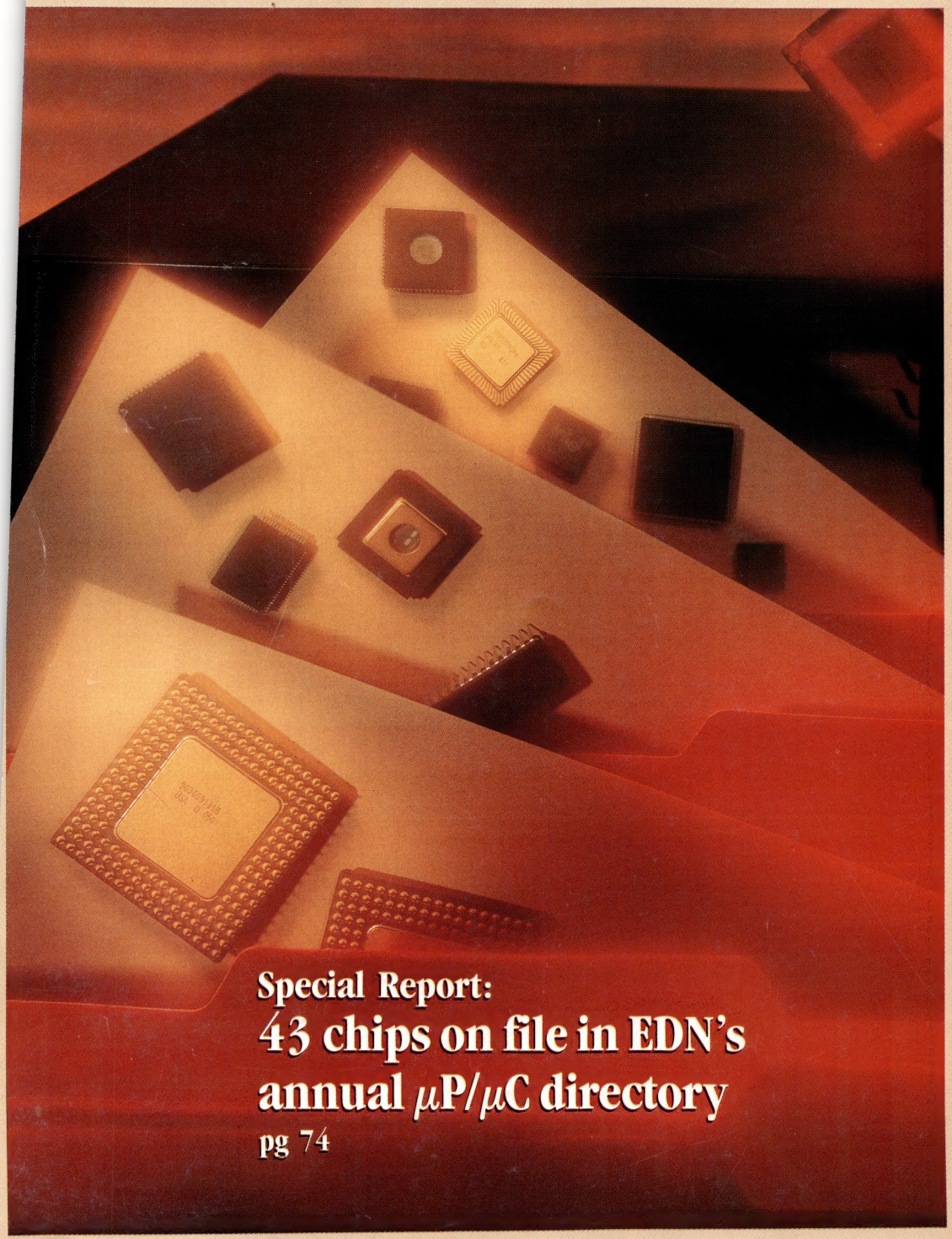
ECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

EDITORIAL QUESTIONNAIRE PG 10

A CAHNERS PUBLICATION

November 26, 1992



Special Report:
43 chips on file in EDN's annual μP/μC directory
pg 74

EDN's Third Annual Innovation Awards

Complete coverage of this year's winners begins on pg 37

SPECIAL REPORT

EDN's 19th annual μP/μC chip directory
pg 74

TECHNOLOGY UPDATE

Analog ASICs make your circuits leaner and meaner
pg 53

You may think your old test equipment isn't worth anything. We think it's worth 20%.

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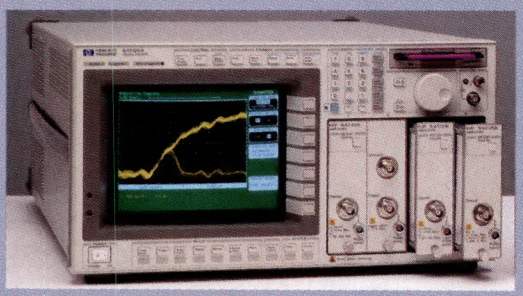

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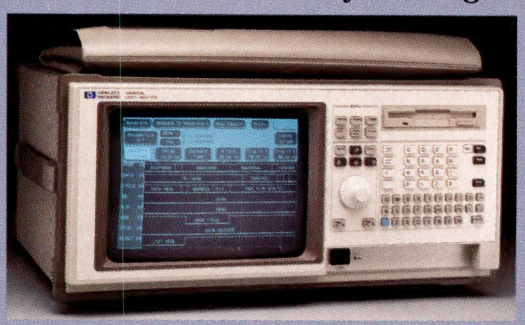

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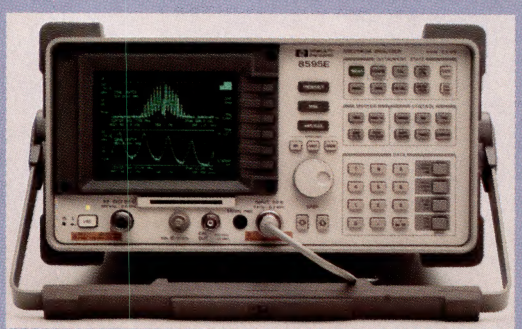

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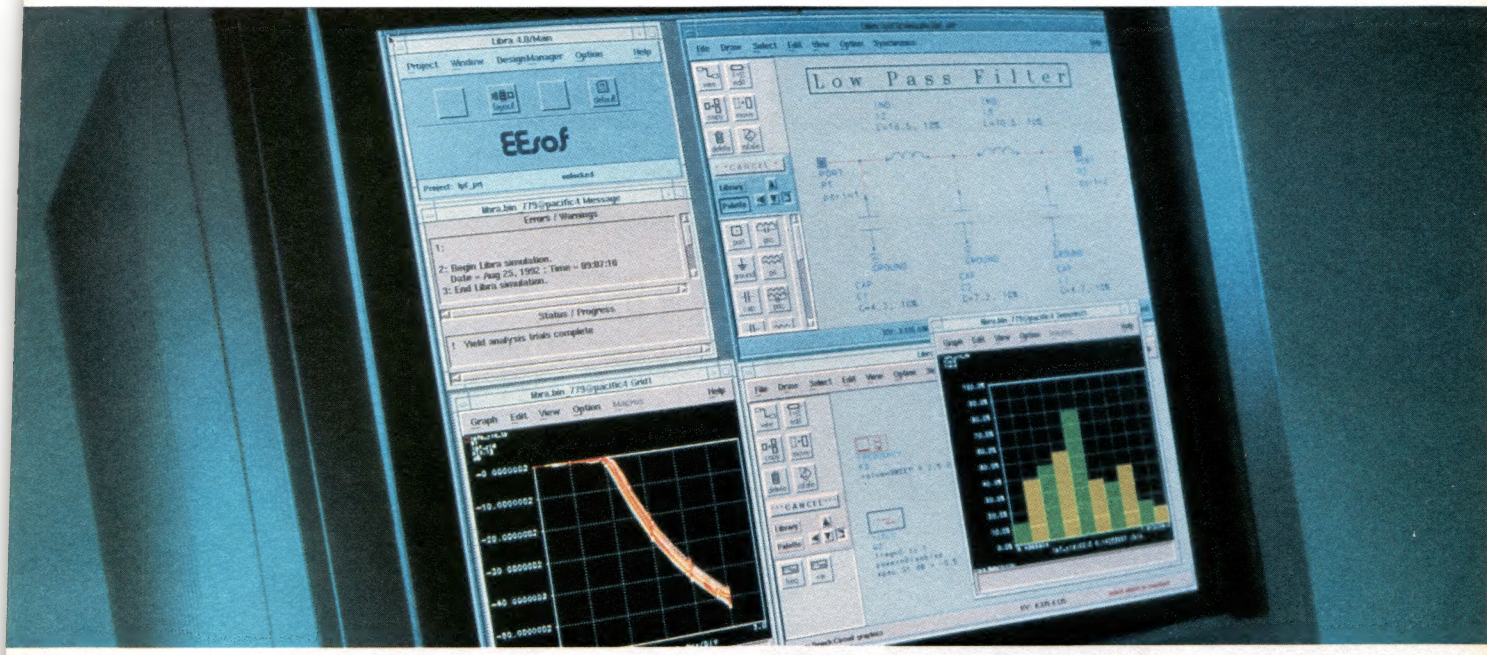

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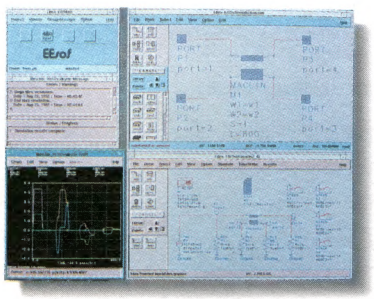

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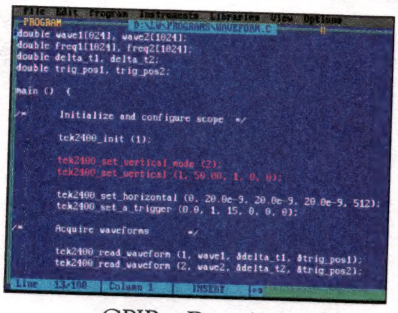

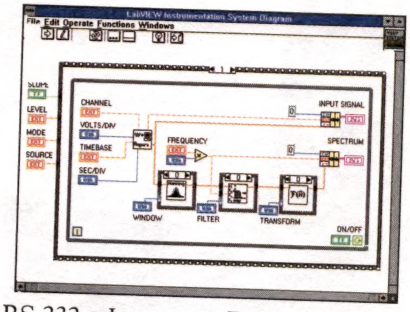

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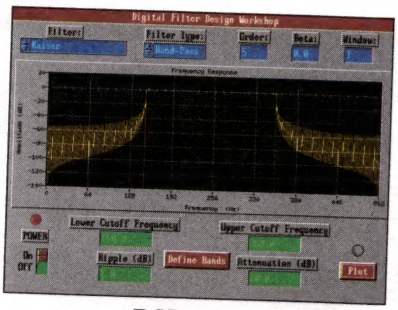

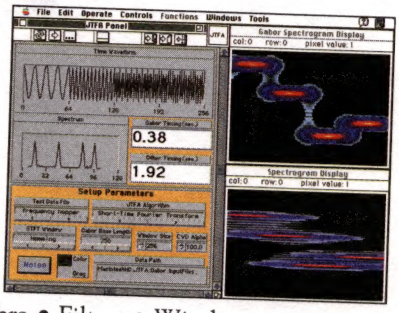

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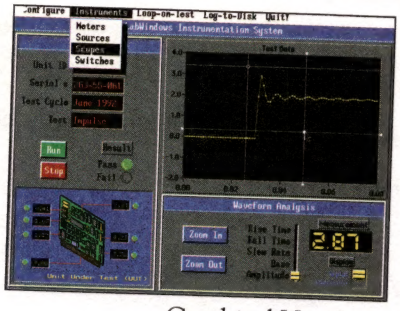

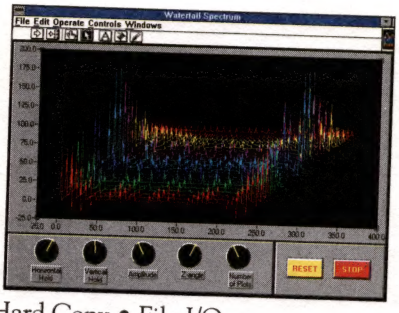

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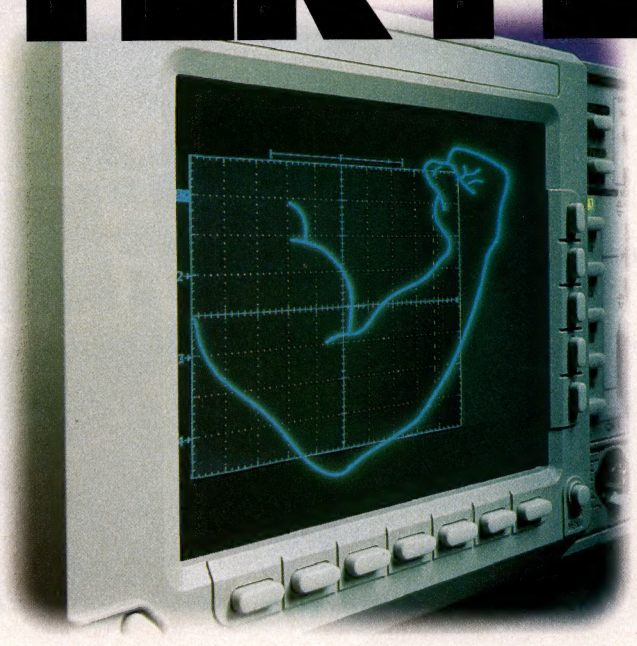

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EDN

November 26, 1992 VOLUME 37, NUMBER 24

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

On the cover: EDN's annual microprocessor directory continues to help organize your μP/μC choices. This year, we've overhauled our format, making comparisons and selections a breeze. Cover photo courtesy Intel Corp; concept and photography by Imagination. . . . . **PAGE 74**

How do we rate?
See our editorial questionnaire on pg 10

Continued on page 7

Foldout Contents

Turn to the last information-retrieval service card in the back of this magazine and you'll find a foldout table of contents. Now, instead of flipping back and forth from this table of contents to the articles you want to read, you can have the convenient foldout open at all times while you're reading EDN. Use the foldout contents to mark off articles you'd like your colleagues to read or to remind yourself to copy stories for your files.

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EDN

November 26, 1992

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EDITORIAL

It's easy to get swept up in the craze of using fashionable words. Let's remember what we want to say, and say it clearly.—*Jon Titus, Editor*

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CIRCLE NO. 8

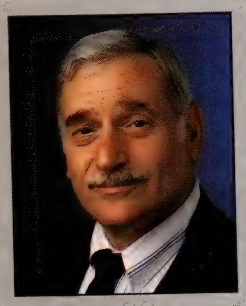
INSIDE EDN

A summary and analysis of articles in this issue

Hard to believe we've been doing the **EDN Microprocessor Directory** for 19 years. When we first published the directory, microprocessors were in their infancy, and engineers were struggling just to get a grip on the devices. "But the nature of the industry has changed, and our directory needed to change with it." So says Ray Weiss, who did just that. Although it might look similar to the directories of yesteryear, Ray has rewritten all 43 entries, making it easier to compare architectures, performance, and prices at a glance.

The results of Ray's and Julie's massive efforts are evident in the 19th annual μP/μC chip directory, which takes up the bulk of this issue. Let us know what you think of the new, revised directory by putting a comment on the reader-service card or sending us a fax at (617) 558-4470.

Like our directory, **analog ASICs** have been around since the 70s. What's been happening in the 90s? John Gallant found out that "analog ASICs are the latest examples of the incredible shrinking IC. You can consolidate as much as a lab bench worth of circuitry into a single chip."



Ray Weiss

Julie Anne Schofield

John Gallant

When he started organizing the directory with Julie Anne Schofield late last winter, Ray had to make some tough choices. Which μPs/μCs had to go? Which to include? "We chose the processors that we see engineers designing-in now and for the rest of the 90s. We dropped some of the processors that people love because, though they're still being used, they're not going into a lot of new design-ins. We did that by talking to companies and designers themselves."

Another tricky job was trying to assign bit sizes—something that seems to defy standardization. For example, looking at the 68000 from a strictly architectural viewpoint, Ray assigned it to the 16-bit category. Our Executive Editor, Steve Leibson (an ex-68000 system designer) later convinced Ray that it was a true 32-bit software architecture.

So, like their digital counterparts, analog ASICs have gotten quicker and denser. But for all its advantages, analog ASIC design is not for the faint of heart. John tells you what to watch out for in his Technology Update.

Finally, we present the results of our **Third Annual Innovator and Innovations of the Year awards.** We tallied up your votes, announced the winners at a black-tie reception at Wescon, and included them in this issue. Thanks for voting, and thanks go to all the nominees in our annual campaign to honor innovation and creativity in the electronics industry.

Joan Morrow Lynch
Managing Editor

HOW DO WE RATE?

During the past year, we've made some changes in EDN, and we'd like to know what you think about these enhancements. Please take a few minutes to answer the following questions. You can mail your answers to **The Editor, EDN Magazine, 275 Washington St, Newton, MA 02158**, or send them via fax to (617) 558-4470. Thanks for your help.

1. I read EDN

☐ 4 out of 4 issues ☐ 3 out of 4 issues ☐ 2 out of 4 issues ☐ 1 out of 4 issues ☐ Don't read EDN

2. Overall, how do you rate EDN's new look?

☐ Excellent ☐ Good ☐ Fair ☐ Poor ☐ Didn't notice any changes

3. How useful are the following new sections?

	Very	Somewhat	Not at all	Don't recall seeing
Processor Update	☐	☐	☐	☐
Acronyms and abbreviations	☐	☐	☐	☐
Ask EDN	☐	☐	☐	☐
Inside EDN	☐	☐	☐	☐
Hands On!	☐	☐	☐	☐

4. How useful are these regular sections?

	Very	Somewhat	Not at all	Don't recall seeing
Special Reports (cover article)	☐	☐	☐	☐
Contributed design articles	☐	☐	☐	☐
Technology Updates	☐	☐	☐	☐
Product Updates	☐	☐	☐	☐
Short Products	☐	☐	☐	☐
Design Ideas	☐	☐	☐	☐
Editorial	☐	☐	☐	☐
Professional Issues	☐	☐	☐	☐

5. Do you like EDN's new cover design, which lets us list more articles, departments, and page numbers than our old cover?

☐ Yes ☐ No ☐ No opinion

6. Does the new color-bar coding on the cover, in the table of contents, and on the articles help make your reading easier?

☐ Yes ☐ No ☐ No opinion

7. Are you familiar with EDN's Bulletin-Board Service (BBS)?

☐ No
☐ Yes, but I've never used it
☐ Yes, I'd log on, but I don't have a computer or modem
☐ Yes, I've logged on

8. If you have used the EDN BBS, do you have any comments about how the BBS works or what we could do to improve it?

9. What technical areas are we NOT covering that we should?

10. What technical topics are we covering too much?

11. Please give us any other comments about our level of technical detail, article selection, organization, etc. We would like your comments.

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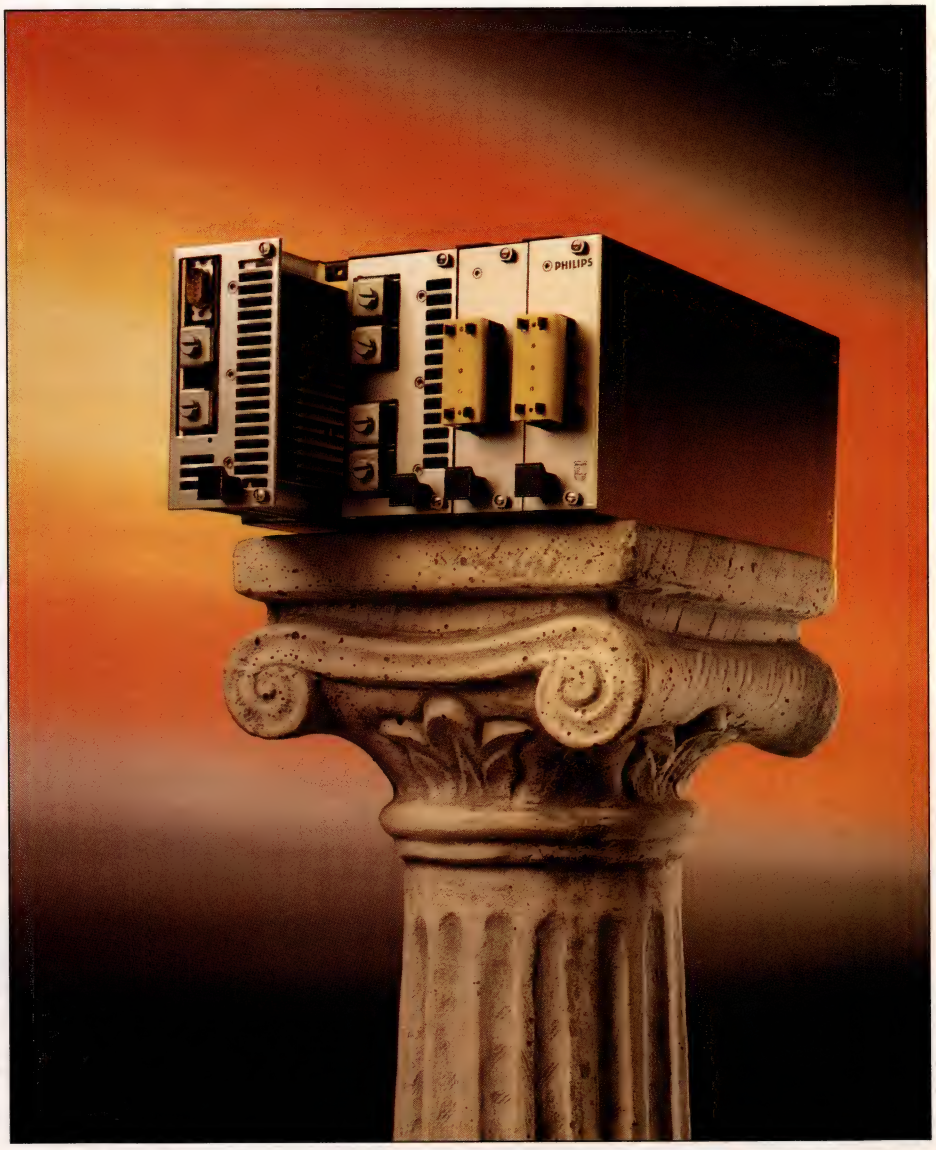

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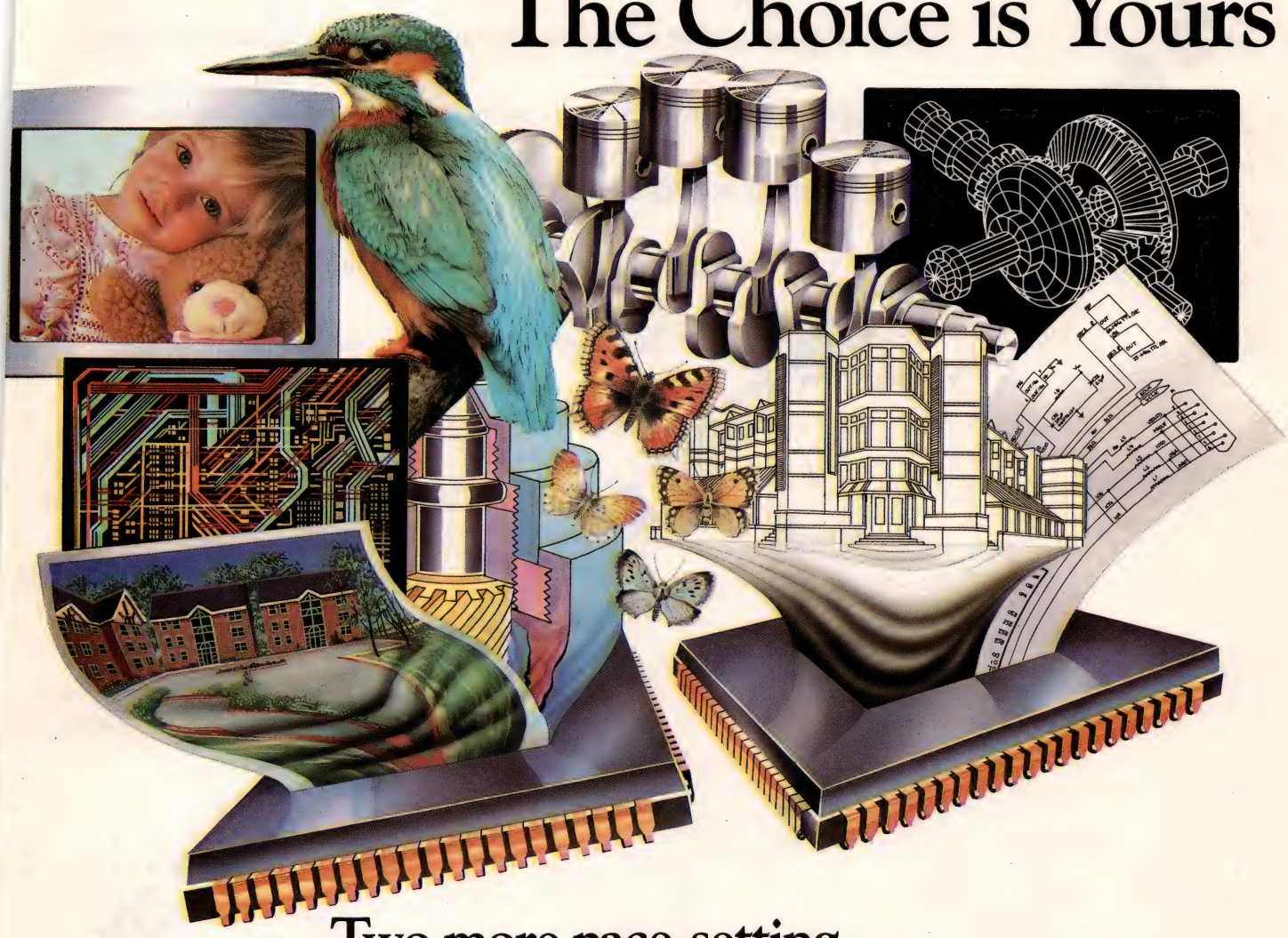

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Two new devices provide today's ultimate solution for high resolution colour or monochrome graphics systems.

TI's TLC34076 provides 16-bit/24-bit true colour, together with: 256 x 24 palette RAM, direct I/F to VRAM, pixel data multiplexing logic, high speed timing logic, and much more.

Available now in speeds of 85, 110 and 135MHz.

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CIRCLE NO. 12

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After all, the volunteer is a member of our new TAS 400 family of analog oscilloscopes. And every TAS has its entire acquisition system (including the vertical, horizontal and trigger functions for each input channel) housed on a proprietary hybrid circuit.

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comes with smashing features like AutoSet, on-screen cursors and readout, dual timebases, and save and recall settings. Plus a unique user interface that makes the 60 MHz TAS 455 and 100 MHz TAS 465 easier to use and dramatically unlike any other analog scope.

A claim that is further backed up by their remarkably affordable price.

But then a lot of performance for not a lot of money is exactly what the TAS is all about. Scopes that add to a long list of low-cost Tektronix products. Like our handheld 60 MHz 224

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new analog scope, we dropped it.

Tektronix
Test and Measurement

CIRCLE NO. 24

The common way to get your PCB designs to manufacturing

You may not be looking for a manufacturing tool that saves you money. But you might be looking for the best layout tool on the market. A tool that can *properly* handle blind and buried vias and is second to none for Analog/Digital PCB, MCM, Flex, Hybrid, or Panel PCB Design. With 2D drafting capabilities that rival mechanical CAD software. A solution with a gridless editor and router for maximum accuracy—all in one package. That's the Zuken solution in a nutshell.

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With Zuken, you can even optimize your assembly process and drive your manufacturing

The Zuken way

tools directly—all with the same user interface. Zuken can also help, even if you're happy with your current front end tools, because our manufacturing tools compliment and interface with all the popular front-end systems. Which is just one more reason why Zuken is the largest PCB workstation software vendor in the world.*

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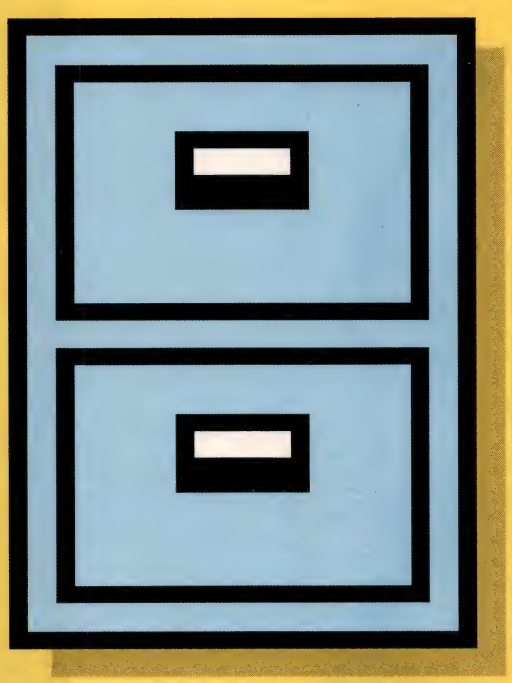
ZUKEN

Manufacturability is Our Objective

CIRCLE NO. 14

What Do These Popula



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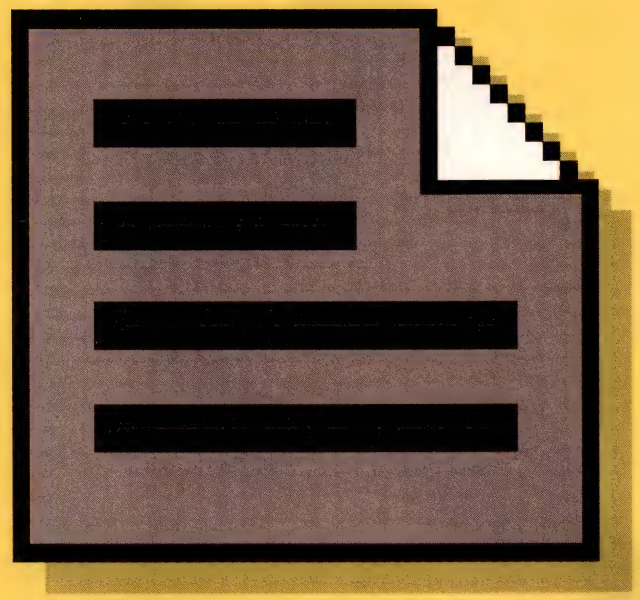
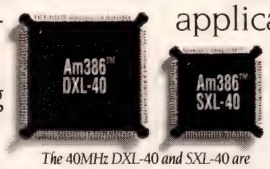


Open a document.

Everyone's getting into Windows.™

And 386-based computers continue to be the popular choice for value-conscious Windows users. The most demanding users—the people who know how to get the most for their money—are insisting on computers built around 40MHz Am386™ microprocessors from AMD.



The 40MHz DXL-40 and SXL-40 are both available in low-cost PQFP packaging.

These are the fastest 386 CPUs made—up to 25% faster in-system than ordinary 386 microprocessors. So they'll run Windows applications the fast and efficient way they were meant to run.

Am386 microprocessors are available in volume. And with AMD's competitive prices, 40MHz 386 machines will come

Windows Icons Mean?

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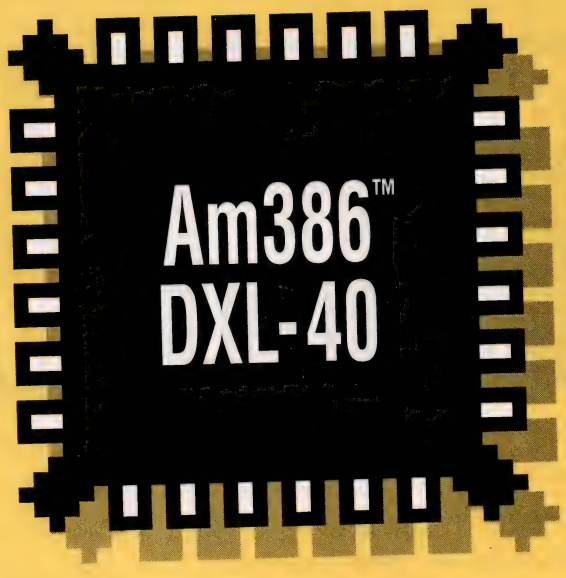

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The Am386DXL and Am386SXL microprocessors are as space-efficient as they are cost-efficient because both are available with PQFP packaging. So holding the line on costs is even easier.

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CIRCLE NO. 15

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THE REST IS HISTORY

CIRCLE NO. 16

EDITED BY SUSAN ROSE

FPGA Update

FPGA offers 7400 to 10,500 usable gates. The 12,320 total gates on Crosspoint's CP21200 provide 60 to 85% usable gates for a typical design. Although the title for highest density FPGA (field programmable gate array) is difficult to assign because of the lack of appropriate benchmarks, the CP21200 is one of the top contenders. Even though the device offers high density, the company claims it is fast enough for applications in systems with clock rates in the 40- to 50-MHz range.

The device has 2240 RAM logic tiles and 8960 transistor-pair tiles arranged in 20 rows with 21 routing channels. Each channel has 38 wiring tracks. Four independent low-skew clock networks provide less than 1-nsec skew across the entire chip and between clocks. You can configure the 196 general-purpose I/O pins as inputs with CMOS or TTL input levels; outputs with 4-, 8-, or 12-mA drive; or bidirectional. Three pins are designated as a JTAG boundary scan port, and four clock pins bring the total to 203 I/O pins. The device will be available in 299-pin pin-grid arrays or 208-pin quad flatpacks.

The device's fine-grain architecture is very similar to standard mask-programmed gate arrays. You use the same workstation-based CAE tools for design entry, synthesis, simulation, timing, and fault analysis that you would use for gate arrays. The company claims the fine-grain architecture is particularly well-suited for use with synthesis tools. Once the logic is designed, you can place and route your design automatically or interactively. Samples will be available in December, and production begins first quarter of 1993. Price for the one-time programmable, antifuse device is $1100 (100). Crosspoint Solutions Inc, Santa Clara, CA, (408) 988-1584, FAX (408) 980-9594.

Motorola joins the FPGA bandwagon. Motorola's Logic and Analog Technology Group have licensed Pilkington Microelectronics' (UK) fourth-generation dynamically programmable-logic-device (DPLD) technology to codevelop an FPGA family. The architecture is intended for sequential-logic register-rich applications. Although the company isn't disclosing details of the architecture yet, they claim the fine-grain Pilkington architecture closely resembles Motorola's sea-of-gates architecture found in its existing H4C family of CMOS gate arrays. The company plans to offer an easy migration path from FPGAs to metal programmed gate arrays. Expect initial sampling by fourth quarter of 1993. Motorola Inc, Mesa, AZ, (602) 962-2597.

FPGA increases speed 33%. AT&T is now producing their ATT3000 FPGA family using a 0.6-μm CMOS process that provides an increased maximum toggle rate from 150 to 200 MHz. The company expects full production by the end of 1992. The ATT3090, in a 160-pin quad flatpack, costs $211 (1000); an ATT3042, in an 84-pin plastic leaded chip carrier, costs $48 (1000). AT&T, Allentown, PA, (800) 372-2447, x856, FAX (215) 778-4106.—by Doug Conner

NTTC opens gateway to federal technology information

The National Technology Transfer Center (NTTC) recently opened a gateway to technical knowledge in the federal laboratory system. A special toll-free telephone number gives US businesses and industries a direct connection to the center's personnel who can access data in 700 federal laboratories. Lee W Rivers, executive director of the NTTC at Wheeling Jesuit College, says "This is not another government data base. Individuals calling 1-800-678-6882 will speak to a person, not a machine. After collecting specifics on each caller's needs, the technology access agents will begin a search of all available databases in the federal government to find answers and solutions." Rivers said the gateway will bring $22 billion worth of annual federal research investment to bear on the drive to increase American competitiveness.

—by John Gallant

Viewlogic ports Unix product to Windows

Last August, Viewlogic Systems ported its EDA tools to Unix with Powerview. In December, 1992, the company will release an equivalent tool set running under Windows 3.1. Workview for Windows has a 32-bit software architecture, and the company will port it to Windows NT when that operating system ships.

The tool set is compatible with the maker's other tool sets, (Powerview and Workview 4.1 for DOS) and will be compatible with the Windows NT version. Major tool components in the set include the Viewframe framework, Viewdraw design entry, Viewsim simulation, Viewtrace design analysis, on-line help, and the Viewscript extension language. Initial hardware requirement is a 25-MHz, 486-compatible PC; the company plans to ease requirements down to 386 machines in later releases. The base configuration costs $7500. Viewlogic Systems Inc, Marlborough, MA, (508) 480-0881, FAX (508) 480-0882.

—by John C Napier

PC-board layout goes under Windows

Running under Microsoft Windows 3.1, TangoPRO pc-board-layout software accommodates large, complex designs. The software is not just a conversion of the company's older Tango product to run under Windows, but an entirely new product. The software uses a 32-bit architecture and database, offering submicron resolution on board sizes up to 60×60 in. The software supports metric designs, too. Components may be placed and rotated

Text continued on pg 22

Data-acquisition and analysis software get GUI

By using the Windows graphical user interface (GUI), SnapMaster for Windows (a data-acquisition and analysis program), lets you create virtual instruments by clicking and dragging icons across your computer screen. Because this program resides in a Microsoft Windows environment, it increases the amount of usable computer memory to 30 times that of DOS and lets you share information between applications. This program also lets you control sensors, transducers, and signal conditioners as part of the data-acquisition process.

Organized into three modules, this package provides data acquisition, general analysis, and frequency analysis. The $995 data-acquisition module facilitates near-real-time plotting, storage, and data retrieval, operating to the maximum speed of your A/D hardware. The $495 general-analysis module lets you construct simple or complex equations by pointing and clicking on the information you need in an equation-builder window. You can develop arithmetic, trigonometric, logarithmic, and statistical functions, along with auto- and cross-correlation, smoothing, differentiation, and integration. The $495 frequency-analysis module converts time-domain data to the frequency domain for analysis, display, storage, and retrieval. HEM Data Corp, Southfield, MI, (313) 559-5607, FAX (313) 559-8008.

—by JD Mosley

Text continued from pg 21

in 0.1° increments. Real-time measurement of trace lengths lets you control critical nets or match them to other nets. Copper sharing lets you T-route nets. The software lets you make solid or hatched copper pours around traces with automatic clearance. If necessary, you can later plow traces out of copper pours. The software uses dialog boxes and menus to help you create pad stacks, blind vias, and buried vias. You can have as many 99 layers and 16,000 pad stacks per design.

The software costs $5950 and is scheduled to begin shipping in January 1993. With an optional rip-up-and-reconstruct autorouter, the price is $10,950. TangoPRO schematic for Windows will follow in the Spring of 1993. You can read current Tango series II design files and pattern libraries directly into TangoPRO without translation. Accel Technologies Inc, San Diego, CA, (619) 554-1000, FAX (619) 554-1019.—by Doug Conner

Windows offered for consumer-level embedded applications

Microsoft is unleashing Windows on consumer-level embedded applications with a product called Modular Windows. The software is based on the company's Windows 3.1 operating-system shell and the underlying DOS operating system. The software runs on 80386-based systems and requires 1 Mbyte each of ROM and RAM. You can use PC-based Windows software development tools to create Modular Windows applications. The only extra software you'll need to create applications is a $99 software-development kit.

To create a modular operating environment for specific applications, the company threw out many of the more general-purpose Windows 3.1 features, such as multiple windowing, printer drivers, and the program manager. The intent was to create a runtime environment that provides device independence for consumer applications. Just as Windows 3.1 makes display and printer variations invisible to the application program, Modular Windows provides a consistent application programming interface for various I/O devices such as a TV screen, keyboard, and joystick.

Because the software is intended for high-volume consumer applications, the company will negotiate licenses for Modular Windows on a company-by-company basis. You can purchase a license outright, but the company will also consider royalties on a per-unit and a per-use basis where applicable. Microsoft Corp, Redmond, WA, (206) 882-8080, FAX (206) 936-7329.

—by Steven H Leibson

Upgradable mother board offers 11 CPU options

Using any of eleven CPUs ranging from the 80386 DX25 to the 80486DX2-66, the 11-in-1 mother board incorporates a clock-circuit design that routes one of four different clock frequencies (25, 33, 40, and 50 MHz) to the processor pad via user-selectable jumpers. In addition, the CPU's solder pad consists of two concentric pads that let it accommodate a variety of processors. The inner pad is sized for the 386 family of processors, and the larger outer pad fits the 486SX CPU family. You install the larger 486DX processors with an onboard upgrade socket. Cache memory sockets let you install a 64-, 128-, or 256-kbyte cache.

The mother board contains six 16-bit and two 8-bit ISA expansion card slots. Eight SIMM sockets let you populate it with as much as 32 Mbytes of RAM. An onboard VESA local-bus connector lets you add high-speed graphics controllers to boost your computer's performance. And the fact that this single $100 (1000) mother board can replace eleven results in lower inventory costs for manufacturers. DataExpert Corp, Sunnyvale, CA, (800) 328-2397, (408) 737-8880, contact Jerry Burns.

—by JD Mosley

Get the Jump on Windowed Environments for Circuit Design!

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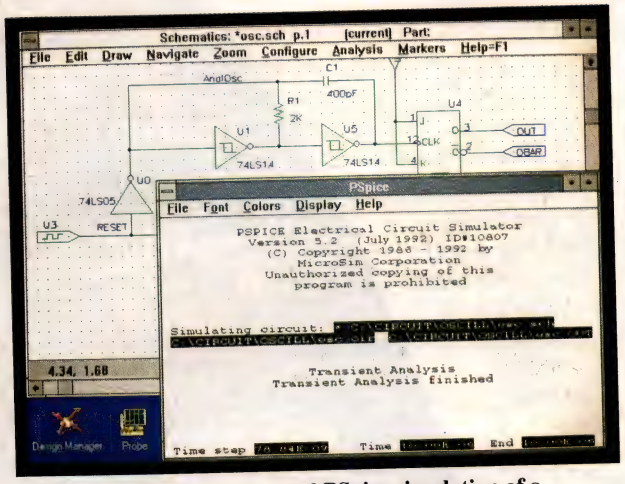
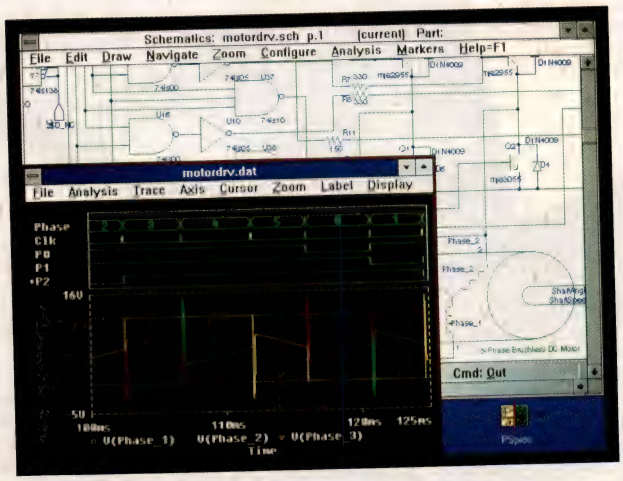


Schematic capture and PSpice simulation of a mixed analog/digital oscillator



Graphical analysis of the analog and digital signals produced by a DC brushless motor simulation

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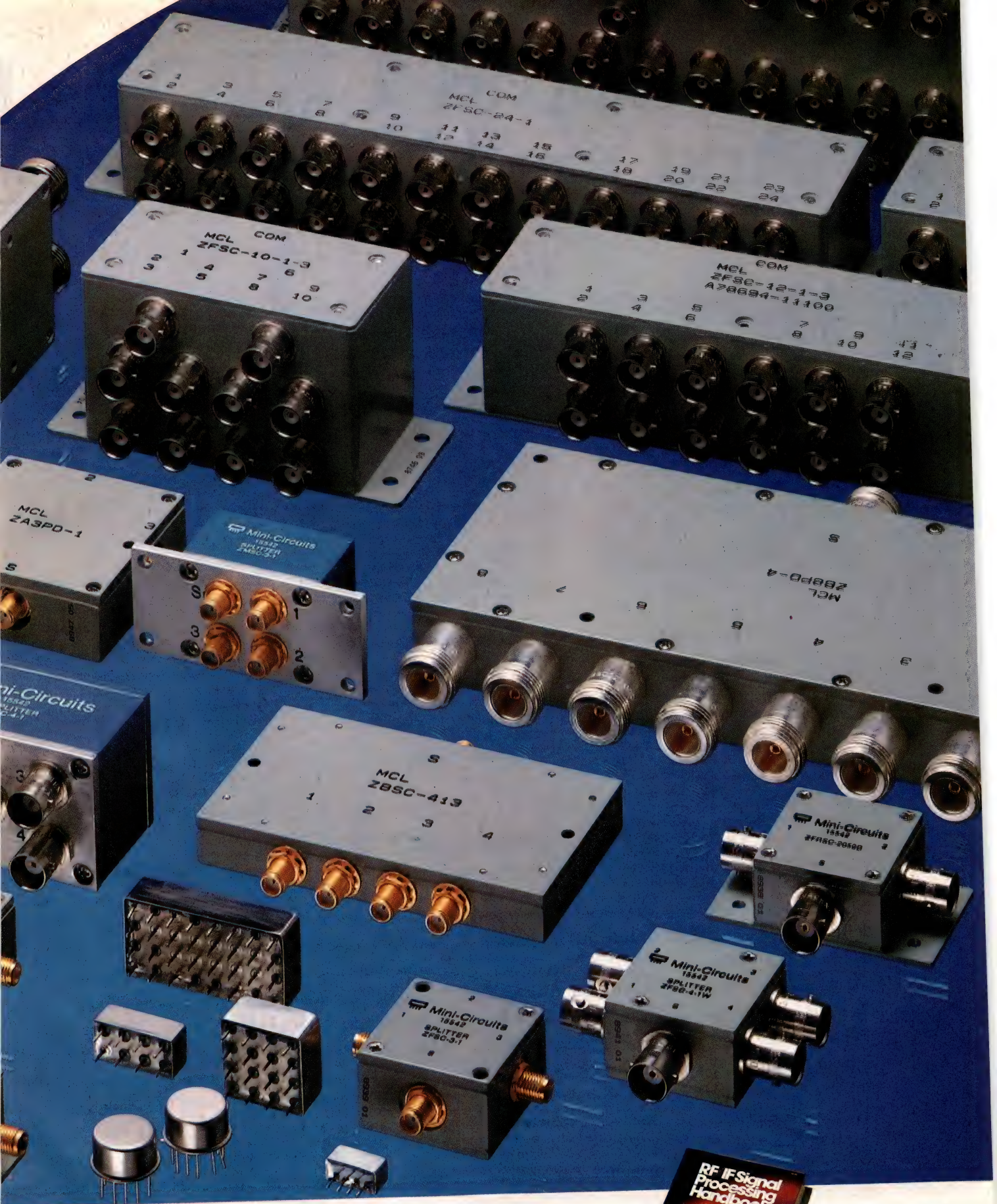

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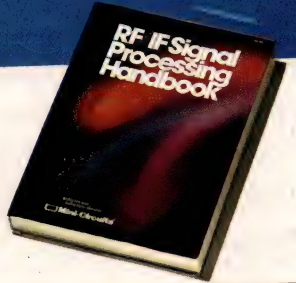

CIRCLE NO. 17

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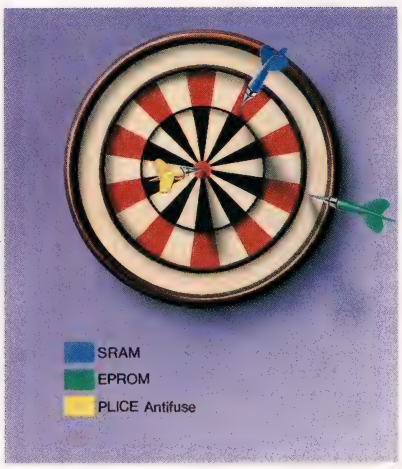

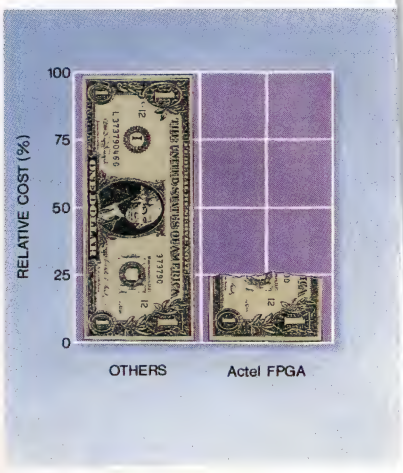

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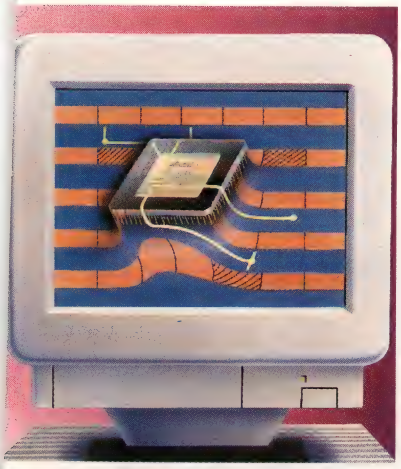

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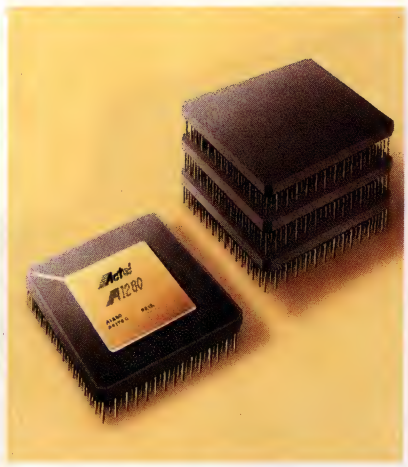

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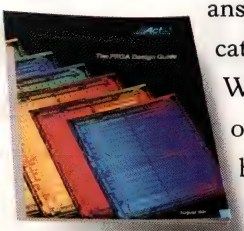

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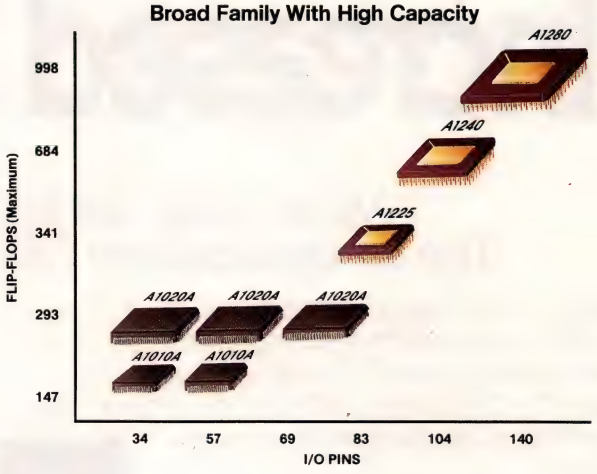

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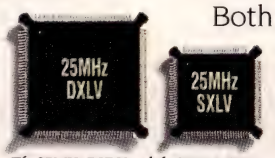
Increased 386 Perform

AMD's 3-Volt 386 Microprocessors Deliver The Longest Battery Life For Portable Computing.

The power struggle continues. While you can get a 386 microprocessor that goes fast, you'll still burn through a battery charge in a hurry. Low-voltage 386 CPUs from AMD are the answer—the Am386™SXLV and Am386DXLV microprocessors.

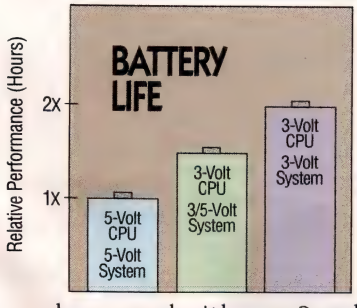
Here are two CPUs made not only to go fast, but to go the distance with portable computer users. Unlike common power-hungry 386s, these low-voltage CPUs run on 3 volts. And they automatically slip into a static "sleep" mode to save power whenever the processor is idle. So users depend less on recharge units—and get the longest operational battery life.



The 25MHz DXLV and the 25MHz SXLV are available in PQFP packaging.

Both Am386 CPUs were designed to fit as comfortably in your budget as they do your portable computers. But you won't compromise on performance because the Am386SXLV and Am386DXLV 3-volt microprocessors both run at 25MHz. So

ance At No Extra Charge.



they're plenty powerful for running Windows.™

Now there's nothing stopping you from charging forth with more efficient 3-volt laptops, notebooks, and palmtops. AMD also has your memory needs covered with our 3-volt EPROMs. And now that the industry at large has welcomed low-voltage portable computing, you'll find the rest of your components equally easy to come by.

For more information on low-voltage 386 microprocessors and support logic, call AMD. And become the current leader in portable computing.

Advanced Micro Devices

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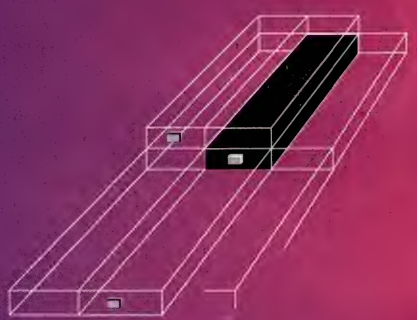
			Charging Current (mA)	Time (Hrs.)	L (mm)	W (mm)	T (mm)	
KF-A600	1.2	600	60	14-16	67.0	17.0	6.1	23
KF-A900	1.2	900	90	14-16	67.0	17.0	8.1	30
KF-A1200	1.2	1200	120	14-16	67.0	17.0	10.3	38
KF-B600	1.2	600	60	14-16	48.0	17.0	8.1	21
KF-B400	1.2	400	40	14-16	48.0	17.0	6.1	16



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SANYO Energy (U.S.A.) Corporation
2001 Sanyo Avenue
San Diego, CA 92173

CIRCLE NO. 20

Watch your language

Over the years, the electronics and computer industries have overused their share of words. Examples include new, unique, powerful, and feature. Recently though, we're hearing people badly misuse words, perhaps without meaning to. It's easy to slip into the habit of applying fashionable terms to the wrong things. I believe we can reverse this trend and get back to language that clearly says what we mean, though. But we've got to make the effort to think about what we're saying. Here are a few examples of what we're up against.

One of the words most often misused today is *paradigm*. It's one of those words that people will always use incorrectly, even if they bother to look it up in the dictionary. It's difficult to be clear on what a paradigm really is. In one dictionary, it's an example or a pattern; in another, an example or a *model*. Often, I've seen it used to mean a particular way of thinking about something. Paradigm is so poorly used, let's banish it and talk and write about examples of thinking, patterns of solving problems, and so on.

Object oriented runs a close second to the word I mentioned above. These days you cannot sell a product—particularly a software product—unless it's object oriented. The first question you should ask is, "What does that mean?" In most cases, object oriented is a throw-away phrase that has been added because it sounds good. As the phrase spreads, power supplies soon will be object oriented. Back in the 70s, products were microprocessorized. These days, they're object oriented. As a youngster, my daughter was object oriented—she'd grab anything she could get her hands on.

Today we don't load software into our computers. Instead, we put it on *platforms*. I always thought that platforms were a lot like loading docks, and that seats for important people were put up on platforms. Here in the US, politicians have "platforms," which are supposed to be ideas and policies. They don't actually have any ideas and policies, they just have platforms. Those loading docks must have gotten microprocessorized and now have a bit of intelligence, but let's continue to call computers computers and leave platforms out of our writing and talking.

While talking about computers, how could I avoid the word *environment*? We no longer write programs, we develop programs in programming environments. Can't we just say that we're using programming tools or programming software? My environment surrounds me, and it doesn't exist on the flat face of a display. Maybe I'm being overly picky, but we should be able to express ourselves properly without resorting to nebulous words that sound interesting, but that are meaningless when we analyze them. Let's hold out for meaning and not today's language fads.

I can hear a vice president of marketing trying to motivate his technical people. "Come on, people, let's get object oriented around here. I want you to get back to your environments and I want to see those platforms cranking out some code. If we don't finish Project X on time, we won't have a pair of dimes to rub together."

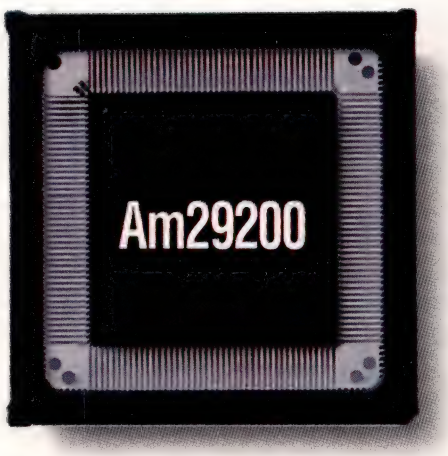
Jesse H. Neal
Editorial Achievement Awards
1990 Certificate, Best Editorial
1990 Certificate, Best Series
1987, 1981 (2), 1978 (2),
1977, 1976, 1975

American Society of
Business Press Editors Award
1991, 1990, 1988, 1983, 1981

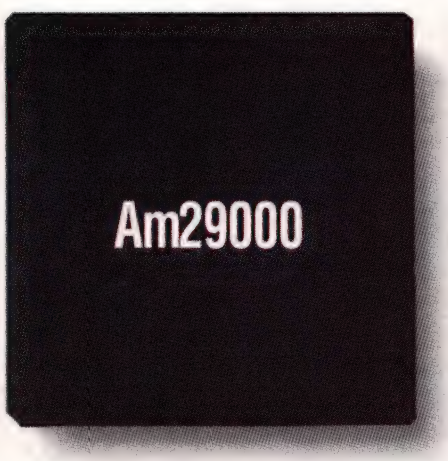
Jon Titus
Editor

Send me your comments via fax at (617) 558-4470, or on the EDN Bulletin Board System at (617) 558-4241 300/1200/2400, 8,N,1; on 9600-bps modems, try (617) 558-4580, 4582, or 4398.

Put These G
And Take So



32-bit RISC microcontroller with integrated peripherals and glueless memory interface.



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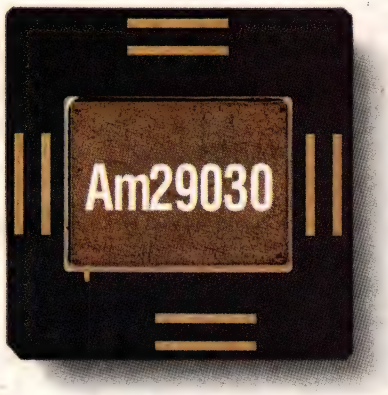
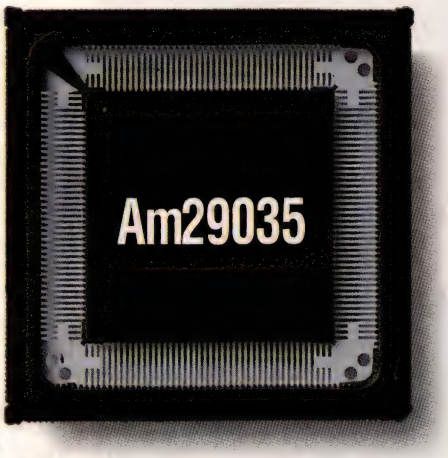
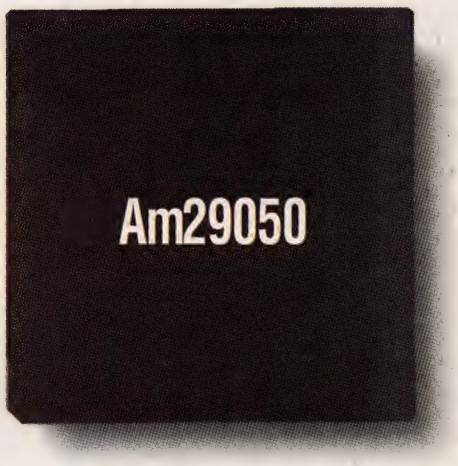
uys To Work
ne Time Off.



32-bit RISC processor with 8Kbyte Instruction cache, Scalable Clocking™ and Programmable Bus Sizing.



32-bit RISC processor with 4Kbyte Instruction cache, Scalable Clocking™ and Programmable Bus Sizing.



32-bit RISC processor with on-chip floating point.

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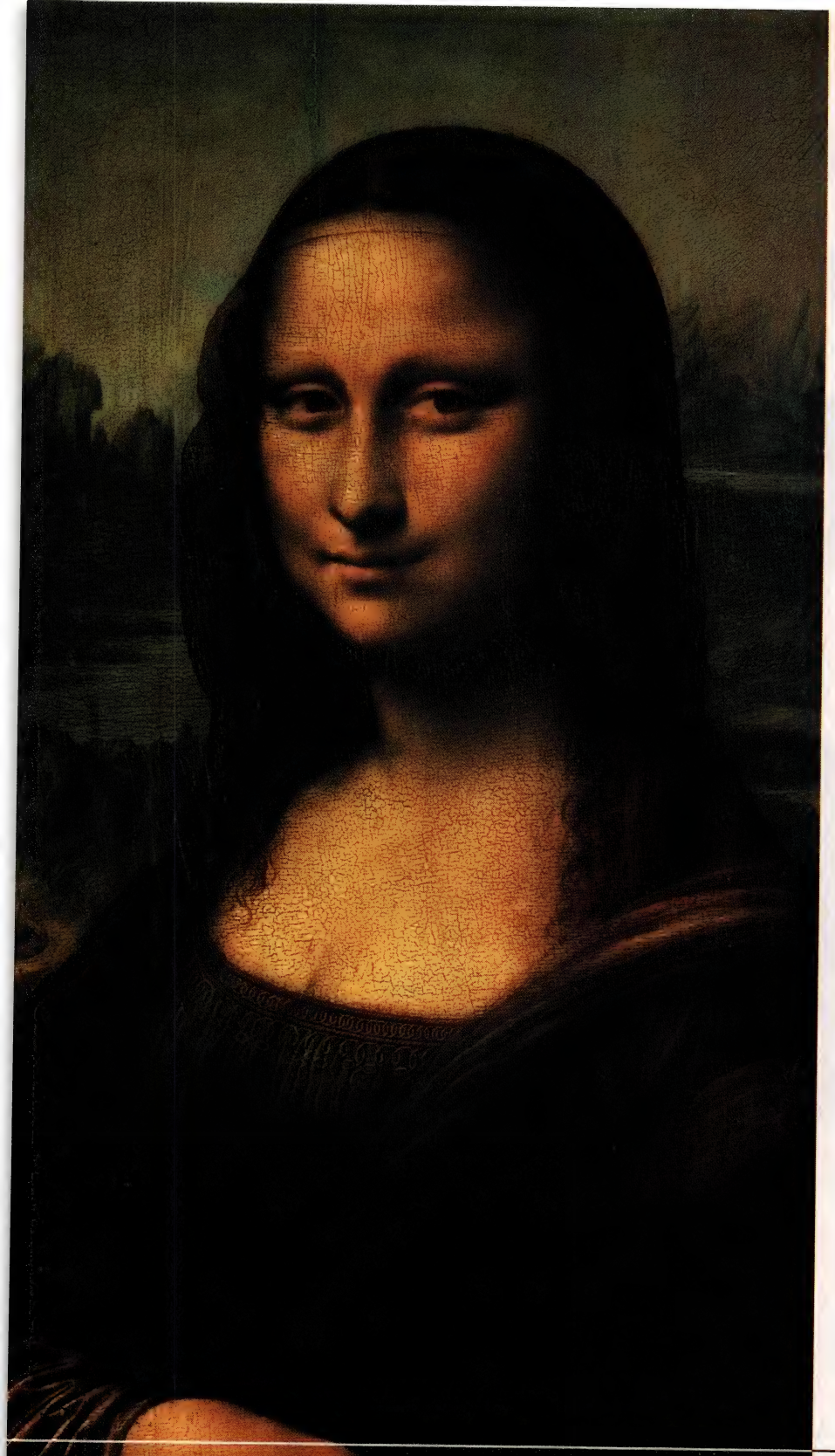
Advanced Micro Devices



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INNOVATION

EDN's third annual Innovator and Innovations Campaign came to a close on Tuesday, November 17 during the Wescon/92 show. EDN honored the Innovation winners and presented their awards at a black-tie dinner. Awards went to one Innovator of the Year and one Innovation winner in each of eight product categories. EDN will present a check for $10,000 in the name of the 1992 Innovator of the Year—Jim Williams—to the university of his choice. All of the winners were selected by votes from EDN readers.

INNOVATOR OF THE YEAR

Jim Williams
Linear Technology Corp, Milpitas, CA

INNOVATIONS OF THE YEAR

SOFTWARE

Gabor Spectrogram
National Instruments, Austin, TX

MICROPROCESSORS

Intel486 DX2 Microprocessor
Intel Corp, Santa Clara, CA

TEST AND MEASUREMENT

90-Series Scopemeters
John Fluke Mfg Co Inc, Everett, WA
Philips Test and Measurement, Eindhoven, The Netherlands

CAE/CAD

DSP Station Software
Mentor Graphics Corp, San Jose, CA

INTEGRATED CIRCUITS AND SEMICONDUCTORS

ADXL50 Acceleration Sensor
Analog Devices Inc, Norwood, MA

COMPUTERS AND PERIPHERALS

Stingray 1842 1.8-in. Disk Drive
Intégral Peripherals Inc, Boulder, CO

COMPONENTS, HARDWARE, AND INTERCONNECTS

AX1024 Programmable Interconnect Device
Aptix Corp, San Jose, CA

POWER SOURCES

3D-PCB Transformer
Philips Industrial Activities SA, Wavre Belgium

EDN wishes to congratulate all the winners and finalists. EDN also thanks all the people who took the time to nominate their products and people. And, as you look over this year's winners, start thinking about who you want to nominate for the 4th annual Innovation Awards. Rules and instructions for next year's competition will be ready by December. To order a nomination kit, Circle No. 347 on our reader service card or fax us at (617) 558-4470.

INNOVATION 1992 INNOVATION WINNERS

INNOVATOR OF THE YEAR

Jim Williams

Linear Technology Corp
Milpitas, CA
Phone (408) 432-1900

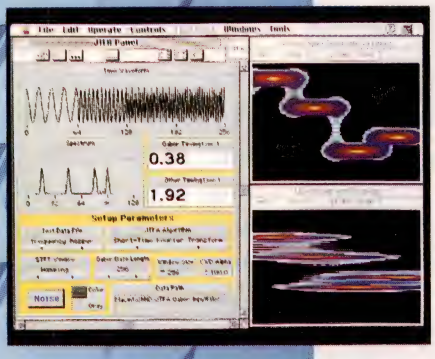
Jim Williams' forte is explaining and popularizing the application of linear-IC technology; the vehicles for his work are application notes, books, and contributed articles in trade journals, including EDN. A recent example is the "Jim Williams papers" on high-speed amplifier techniques. Jim is a staff scientist at Linear Technology. Last year, Linear Tech published a more comprehensive version of the high-speed amplifier series as a 132-page application note.

You might not think that explaining and popularizing a technology involves innovation, but Bob Dobkin, Linear Tech's vice president of engineering, convincingly argues otherwise. In nominating Williams, Dobkin writes, "The innovation in this process lies in identifying problems a customer will face and then finding and sharing the solutions." Without Jim's advocacy to the design community—and that of a dedicated cadre of applications professionals throughout the industry—many promising technologies would languish as laboratory curiosities.

Jim championed the notion that, to be successful, a manufacturer must offer its customers the solutions it has discovered to the problems the customers will face in using the manufacturer's products. Williams says that customers confront three classes of problems: cost constraints, technical difficulties, and design freedoms. When vendors offer advice, they must keep that context always in mind. To solve problems, Jim says, "you have to stick yourself in your customer's shoes."

SOFTWARE WINNER

Gabor Spectrogram



National Instruments
Austin, TX
(512) 794-0100

The Gabor Spectrogram represents a signal's power spectra in the joint time-frequency plane. The spectrogram gives up to twice the resolution of an equivalent short-time Fourier transform (STFT) and runs six times faster due to its greater computational efficiency. National Instruments announced this algorithm at the March 1992 International Conference on Acoustics, Speech, and Signal Processing and includes it in the $1995 Labview for Macintosh and $1495 Labwindows for DOS Analysis Libraries.

The company developed this spectrogram by first applying its own "orthogonal-like" Discrete Gabor Transform (DGT) to a signal, followed by the pseudo Wigner-Ville Distribution (PWVD). The DGT and the PWVD have been known for decades but have seen limited practical use because they are difficult to implement. The company's "orthogonal-like" DGT resolves difficulties with the DGT in the selection of basis functions and auxiliary window functions. In addition, combining the DGT with the PWVD removes some of the PWVD's liabilities.

The DGT decomposes a signal into a linear combination of time-shifted and frequency-modulated Gaussian basis functions. Gaussian basis functions require fewer spectral coefficients than does the STFT, which makes it easier for your computer to perform a DGT. The PWVD also gives better joint time-frequency resolution than the STFT. But the PWVD suffers from mathematical artifacts that lack physical interpretation, such as cross-term interference and negative terms. By using the DGT with the PWVD, the spectrogram separates the artifacts from the useful terms. The spectrogram also allows precalculating the PWVDs of the basis functions and storing them in a lookup table, making computation faster than the equivalent STFT.

You use the spectrogram for analyzing time-varying signals where simultaneous time-frequency results are necessary. Applications include speech processing and recognition, image processing, synthetic music, seismic exploration, sonar, radar, acoustics, vibration analysis, medical imaging, data compression, and computerized vision.

MICROPROCESSOR WINNER

Intel Corp
Santa Clara, CA
(408) 765-8080

Intel486 DX2 Microprocessor

The Intel486 DX2 microprocessor runs at 50 MHz but uses a 25-MHz CPU bus. Thus, the chip can boost system performance with out requiring you to design an entire system for high-speed operation.

Like its Intel-486 DX predecessor, the Intel486 DX2 comprises an integer unit, a floating-point unit, and an 8-kbyte cache. An on-chip PLL circuit uses the external system clock as an input and produces a faster internal clock. A 3-layer metal process lets the core CPU run at 50 MHz, which is twice the speed of the CPU bus.

The processor's integer performance is 40.5 MIPS (V1.1 Dhrystones); its overall SPECmark rating is 19.2 (SPEC '89). The device uses a system-management mode for overseeing system power consumption as well as for implementing suspend-and-resume operation. DOS and Unix are among the operating systems ported to the processor. The device comes in a 168-lead pin-grid array and costs $517 (1000).

TEST AND MEASUREMENT WINNER

John Fluke Mfg Co Inc
Everett, WA
Philips Test and Measurement
Eindhoven, The Netherlands
(800) 443-5853;
(206) 356-5500

90-Series Scopemeters

In packages that measure 2.4 × 5.1 × 10.2-in. and weigh 4 lb (with batteries), the 90-series Scopemeters provide all the measurement functions many engineers need. The units act as 2-channel digital storage oscilloscopes (DSOs) with 50-MHz repetitive-signal bandwidth and 4-digit multimeters (DMMs). The 97, which has an electroluminescent back-lit display, also includes a sine/square-wave generator. Prices range from $1195 to $1795.

Although these instruments are not the first small scopes with LCDs, they are the first with such displays to offer so many features. The features include a 3000-count DMM. The DMM, which resolves >4000 counts without overloading, shares its input leads with the scope's channel A. Scopes that make cursor measurements also provide numeric readouts, but few of them can indicate such quantities as an ac waveform's rms value; these units can. Moreover, few scopes include a calibrator—as these units do—to ensure 3⅔-digit accuracy of their cursor measurements.

Most DSOs of even moderate bandwidth are ac powered and fan cooled. These units use so little power that, not only can they be convection cooled, they are sealed against moisture (they aren't waterproof, however). Furthermore, the units' low power consumption lets them run for four hours before their NiCd cells need recharging. If you don't have access to ac for battery charging, you can replace the NiCd cells with C-size alkaline cells.

Inputs that are isolated from the chassis are commonplace in high-quality digital meters, but you won't find such inputs on most scopes. As a result, measuring waveforms in the presence of high common-mode voltages subjects operators to the possibility of a lethal shock. To provide protection in such applications, the Scopemeters' inputs withstand 600V rms with respect to the case. Using the model 97's RS-232C port to, say, send a waveform to a recorder, doesn't defeat the isolation; the port is optically isolated. The serial-interface cable includes an optical-to-electrical converter powered from the receiving device's RS-232C port.

The most novel technology embodied in the units relates to their measuring capabilities. An 8-bit ADC digitizes the signals for both the waveform and numeric displays at a rate of 25 Msamples/sec. The numeric display uses digital-signal-processing (DSP) techniques implemented in a proprietary IC (one of two in each instrument) to convert the ADC's 8-bit output to a resolution equivalent to approximately 13 bits. DSP techniques also extract the rms values of ac waveforms. On the 95 and 97, you can also obtain readouts in dB and watts.

INNOVATION 1992 INNOVATION WINNERS

CAE/CAD WINNER

DSP Station Software

Mentor Graphics Corp
San Jose, CA
(503) 685-7000
European Development Center
Leuven, Belgium
(32) 16-203063

The DSP Station software performs top-down design of DSP systems from high-level specifications through simulation and optimization from multiple physical implementations. The software provides analysis tools that address the needs of the DSP designer, such as noise and stability analysis, area vs bandwidth tradeoffs, and frequency-domain sensitivity analysis.

DSP Station also helps you plan development and production times for your proposed DSP system and analyze cost/performance ratios. For fast implementation, you can use the software to generate assembly code for a commercial DSP chip. For quick prototype development, you can synthesize a design for a gate array or an FPGA. For the best cost/performance ratio, you can use high-level synthesis to create designs for standard cell module generators. DSP Station lets you use a common input format to drive all the implementation paths.

The software also helps you analyze hardware/software tradeoffs, as well as analog/digital partitioning, from the early phases of design. It also lets you compare various system architectures.

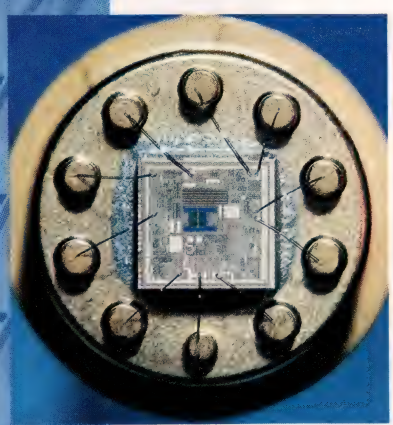
The package includes three forms of synthesis: filter designs, assembly language code for programmable DSPs, and DSP architectures for custom integrated circuits.

The filter design synthesis uses arithmetic optimization techniques in addition to the normal filter approximation routines. Assembly language synthesis uses optimizing techniques to map all your DSP functions onto the particular architecture of the target programmable processor. Silicon synthesis utilizes either bit-serial or bit-parallel modules configured in an optimal design based on scheduling for each signal processing task.

The product, which starts at $33,000, represents a cooperative development effort of a university research lab (Interuniversity Microelectronics Center), an industrial customer (Philips), and a commercial CAE vendor (Mentor Graphics Corp).

INTEGRATED CIRCUITS AND SEMICONDUCTORS WINNER

ADXL50 Acceleration Sensor



Analog Devices Inc
Automotive and Sensor Products Group
Norwood, MA
(617) 461-3557

The ADXL50 acceleration sensor combines a surface-micromachined capacitive sensor with on-chip signal-conditioning and self-test circuitry. The sensor can gauge collisions, judge inertial positioning, and monitor active systems. Its primary application is automotive air-bag systems.

Surface micromachining is a process for making silicon structures that can move. Multiple thin films—as well as layers of silicon and silicon oxide—are deposited and etched to produce movable parts with dimensions of 1 to 2 μm. This process lets electronic circuitry and micromachined structures reside on the same chip.

The ADXL50 measures acceleration in a single plane of sensitivity over the ±50g range to an accuracy of 5%. Unlike accelerometers that monitor the resistance changes of stressed piezoresistors to detect acceleration, the ADXL50 measures changes in capacitance and is therefore insensitive to temperature changes.

The signal-conditioning circuitry provides excitation signals for the sensor and amplifies the analog output signal. The ADXL50 comes in a 10-lead TO-100 can and costs $23 (100). The sensor is also available in other package styles, and it costs $5 in automotive OEM quantities.

COMPUTERS AND PERIPHERALS WINNER

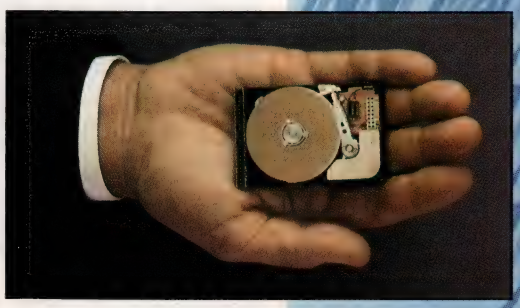
Stingray 1842 1.8-in. Disk Drive

The Stingray 1842 1.8-in. disk drive holds 40 Mbytes and can withstand 300g nonoperating shocks. The dual-platter drive is approximately half the size of a single-platter 2.5-in. drive. With the electronics mounted to the head-disk assembly, the drive measures $76.85 \times 50.8 \times 15$ mm and weighs 3.2 oz.

The drive's many features let it meet the rugged requirements of mobile computing. For example, in most drives, the heads drag along the disk surface when the spindle motor stops. Repeated head takeoffs and landings result in friction-induced damage to the head-disk-assembly interface and can cause long-term reliability problems. In contrast, the Stingray 1842 uses a ramp loading and unloading mechanism to prevent the heads from touching the media.

Because the heads don't slap the disk during power-down, the drive can resist a 300g nonoperating shock. During power-down and inactivity periods, the spindle motor's back EMF ensures that the heads are securely loaded and locked on the ramp structure. During power-up, a microprocessor determines when the spindle motor is up to speed before reading the servo bursts and calibrating the heads to read and write data.

The dynamic ramp-loading mechanism lets the drive spin down to sleep mode as many as 1 million times. The drive consumes 15 mW in sleep mode and can recover from this mode in approximately 1.5 sec. Because the heads do not drag on the media, spin-ups and spin-downs are faster and consume less power than those of conventional drives.



Other specifications include an 18-msec access time, 0.8A start-up current, 3571-rpm spindle speed, interface transfer rate of 4.0 Mbytes/sec, media transfer rate as fast as 1.9 Mbytes/sec, -40 to $+70$°C operation; and a 100,000-hour MTBF. The drive costs $285 ($1000 per month OEM).

Integral Peripherals Inc
Boulder, CO 80301
(303) 449-8009

COMPONENTS, HARDWARE, AND INTERCONNECTS WINNER

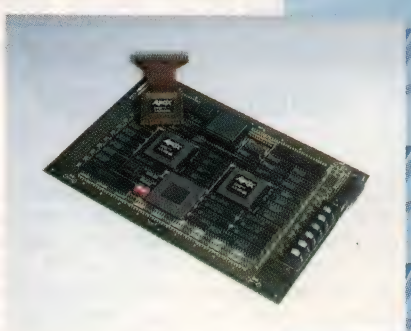
AX1024 Programmable Interconnect Device

The AX1024 field-programmable interconnect components can create a resistive circuit path between any two of 940 inputs and outputs. Each device has a RAM-based programming scheme that enables you to reprogram device connections on the fly.

A programmed connection uses a pass transistor to electrically join two of the I/O pins. Once activated, the pass transistor stays on, making the bandwidth of the AX1024 interconnect independent of the transistor's switching speed. Signals sent through the interconnect device must stay between 0 and 5V, but they do not have to conform to any logic levels; they can even be analog signals.

The interconnect device is available in two versions. In addition to its 940 interconnect pins, the $2938 AX1024D provides 64 diagnostic pins on an attached flex cable. The device package features spring-loaded connecting pins and is intended for prototype troubleshooting.

The $1105 AX1024R has no diagnostic pins. This unit is housed in a more conventional surface-mountable pin-grid array. Both of these devices connect to a pc board using a 32×32-pad array spaced on 40-mil centers.



You need software to make these programmable devices useful. The development software currently available runs on SPARCstations and costs $15,000. The company plans to announce PC software shortly. Two prototyping boards are available that will help you use the AX1024 devices.

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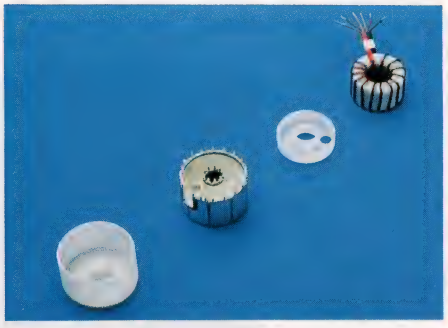
3D-PCB Transformer

The 3D-PCB transformer facilitates the design of the magnetics section in high-frequency switching power supplies. Rather than rely on traditional core designs, the unit uses a segmented design,



resulting in much lower leakage inductance values.

Transformer construction uses a ferrite core in the form of a torus with a center hole. The primary winding is wound directly around the core. The secondary winding is made up of a number of electrically conductive segments. These segments, which are formed somewhat like U-shaped plates, feature mounting pins that you solder to a pc board. The transformer is not fully assembled until the secondary segments have been soldered to the board.

All segments are metallized portions of the outer surface of a cap made from an electrical insulating material, such as plastic. The design integrates one plastic cap for the earth shield, the secondary insulation provided by the plastic cap itself, and several turns of secondary windings.

You can connect the secondary turns in series, in parallel, or in series-parallel combinations via connections on the pc board. Thus, you can tailor the transformer to provide output-voltage and current values to satisfy many user-specific applications. The 3D-PCB transformer is currently being used in a line of 300W supplies. Because the unit is a custom design, prices depend on user requirements.

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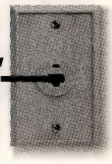

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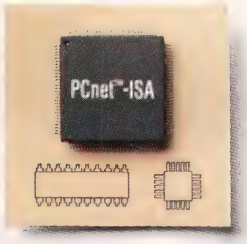

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CIRCLE NO. 27

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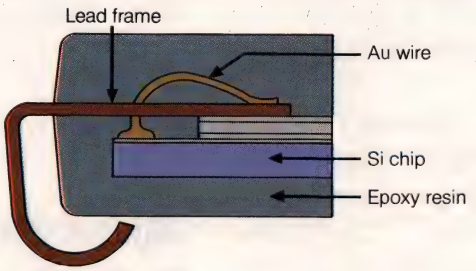

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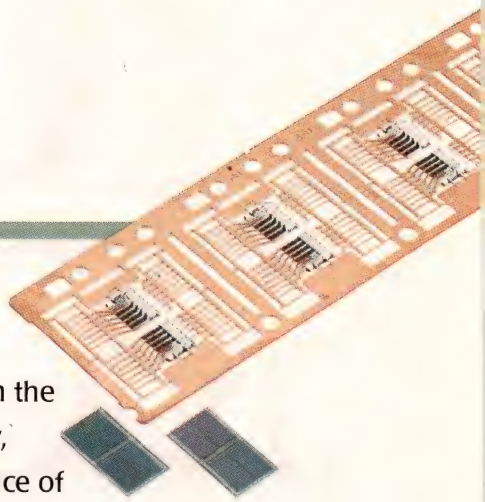

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CIRCLE NO. 13

Can Your Current MCUs Meet These Specs?

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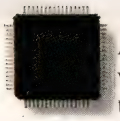
Lowest Power Dissipation

Low Voltage

Largest Memory

Smallest Packages



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CIRCLE NO. 28

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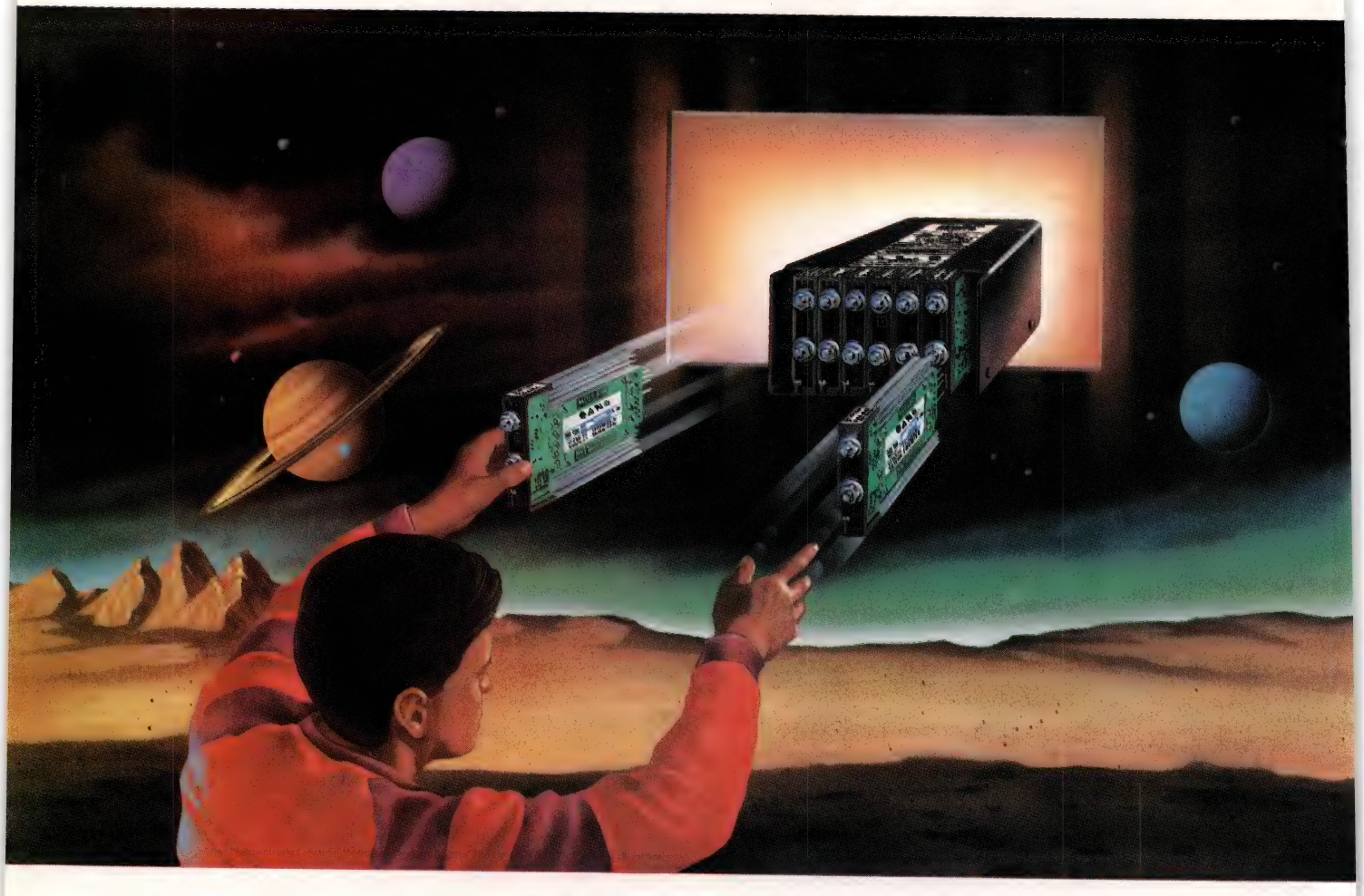

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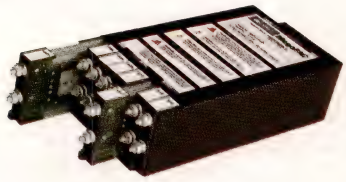

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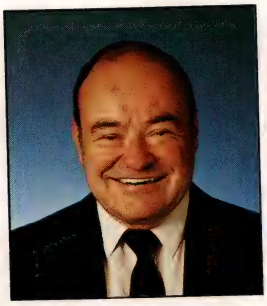
Component Solutions For Your Power System

CIRCLE NO. 29

Analog ASICs make your circuits leaner and meaner

John Gallant, Technical Editor



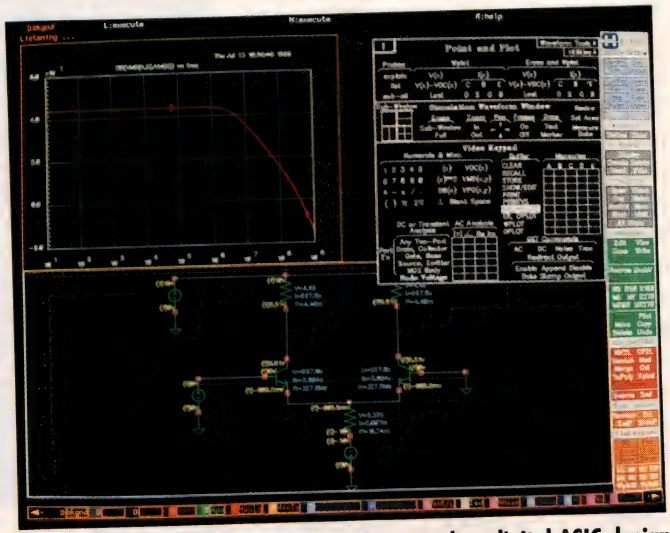
So, your pet analog project is extending beyond the bounds of your lab bench. Why not consolidate that rat's nest in an ASIC?

Analog ASICs not only conserve precious space, they also provide other design benefits. Because on-chip circuit dimensions are smaller and more tightly controlled than circuit-board dimensions, parasitic and high-frequency capacitive-loading effects are less pronounced. Also, similar devices on a single wafer have tighter matching characteristics than their discrete counterparts.

In addition, most analog ASICs have more transistors than you'll know what to do with. The extra transistors let you lavishly sprinkle extra features in your design at minimal cost. In fact, after NRE charges and the cost of development tools, large-quantity custom or semicustom chips are cheaper than circuit boards having multiple components. But analog ASIC design is not recommended for the novice circuit designer. Process limitations create pitfalls that aren't encountered in discrete designs. To be successful, the customer must work in close cooperation with an analog ASIC vendor to avoid falling from dangerous cliffs along the way.

The arrays mentioned in this article are primarily positioned for analog applications. Although many of the arrays also feature digital logic cells, a mixed-signal design based on these ASICs should have an analog emphasis that may require some digital control. A variety of mixed-signal ASICs, such as NCR's VS700 standard-cell array (see **Table 1**), have analog design capabilities also. However, this class of mixed-signal ASIC belongs to applications that have a digital emphasis that require some real-world analog interface, such as op amps, S/H circuits, ADCs, and DACs (an article tentatively scheduled for 1993 will cover these mixed-signal ASICs).

Depending on your expertise, you have a number of options available to develop a custom or semicustom analog ASIC. A semicustom design generally consists of the customer interconnecting a number of predefined building blocks using CAD tools. A custom design consists of a mixture of predefined building blocks and specially designed blocks usually created by the vendor from raw silicon. On one end of the spectrum, standard cells let you interconnect build-



Analog ASIC design tools are as sophisticated as digital ASIC design tools. The Harris Fastrack design system includes tools for device design, device test, simulations, and statistical analysis.

ing blocks from a library of analog macros. Typical analog macros consist of op amps, low-noise amps, S/H circuits, mixers, comparators, bandgap references, and similar complex analog components.

On the other end of the spectrum are tile arrays. Tile arrays consist of one or more sections on a silicon substrate called tiles. Each tile contains an assortment of discrete-level building blocks, such as npn and pnp transistors, JFETs, resistors, capacitors, diodes, and zener diodes. Although tile-array vendors also provide a collection of analog macros, the access to discrete-level devices offers considerable flexibility. However, to take full advantage of tile-array components, the ASIC designer must be well-versed at discrete-level analog design. If you don't know what current mirrors, high-impedance loads, composite npn transistors, or push-pull drivers are, you're probably best advised to use analog macros in standard cells.

Standard cells simplify designs

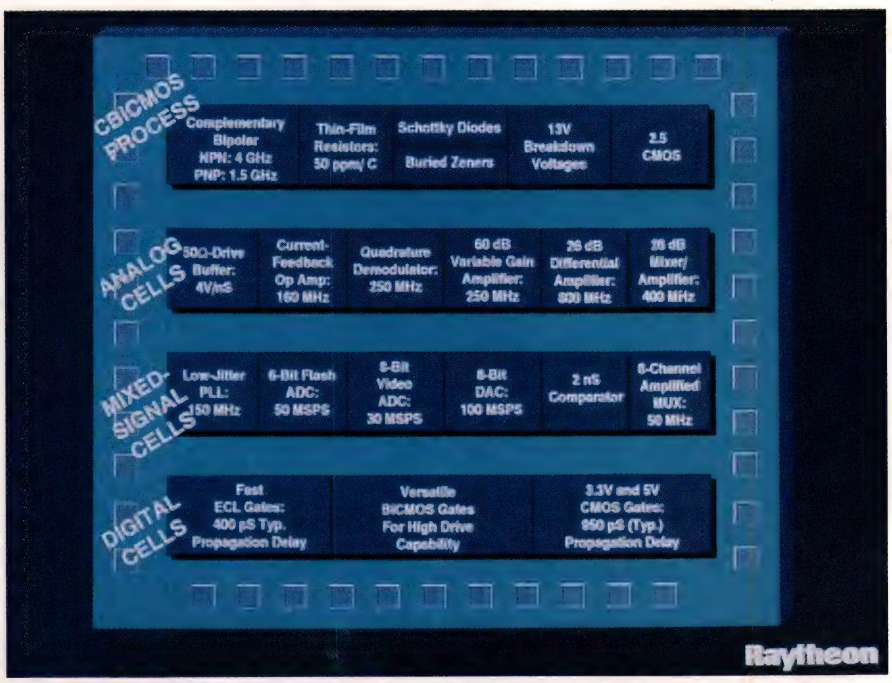
Raytheon's RSC4000 array and Harris' HDI family of arrays are typical standard cells for analog ASICs. The RSC4000 is the latest member of the company's VRSA-Tile family of analog ASICs and consists of complementary bipolar and CMOS (CBiCMOS) devices. The library has 27 analog macros and 37 ECL and CMOS digital macros to implement an analog or mixed-signal design. Analog macros include a 35-MHz general-purpose op amp, 2.5-nV/$\sqrt{\text{Hz}}$ low-noise amp, 160-MHz current-feedback amp, 500-MHz buffer, 3-nsec ECL comparator, 50-MHz 8-channel multiplexed video amplifier, 150-MHz PLL, and a 2.5V bandgap reference. Digital macros include gates, inverters, buffers, flip-flops, latches, TTL-to-ECL translators, and multiplexers. Typical device breakdown voltage is 13V.

To develop a circuit on a chip, you select the appropriate macros from the standard cell library and interconnect them. When the functional design is complete, you capture the schematic on a DOS-compatible computer or a Sun workstation using OrCAD or Cadence's Edge or Artist schematic-capture packages. You can simulate the design using PSpice or HSpice and, if the digital portion is significant, you can use Cadence's Verilog simulator. When the simulation runs are satisfactory, you finalize the schematic and generate a detailed electrical specification for the ASIC. It is also important that you develop a detailed test strategy, including temperature tests, that completely tests both the analog and digital sections of the ASIC.

Once the design and test plan are complete, you submit the design package to the standard-cell vendor you are working with for design review. During the design review, a mutual agreement is reached on the final schematic and specifications for the device. For example, for Raytheon's RSC4000 ASIC, the company's design engineers rerun the simulations and resolve any discrepancies. Agreement is also reached on the test requirements for the device. Raytheon then produces the mask layers to produce a number of prototype devices for customer test. This design procedure is typical for all of the standard-cell vendors. In fact, all of the vendors emphasize that close customer and vendor cooperation is the key to first-silicon success.

Isolation approximates discretes

The Harris HDI family of standard cells provides a marriage between 26 predefined analog macros and a library of active and passive discrete components. In addition, the inclusion of hard-coded macrocells lets you modify the device-level transistors and components in specific analog macros. The key to this added flexibility is dielectric isolation. Each transistor in the analog array is encircled by a dielec-



Standard cells let you interconnect complex analog macros to design an analog ASIC. Raytheon's RSC4000 complementary BiCMOS standard cell contains 27 analog and 37 digital macro cells to accomplish an analog or mixed-signal design.

Table 1—Representative analog-ASIC tile arrays

Company	Model	Family type	Breakdown voltage	Transistor f_t (GHz)	Macros	Design platforms	CAD tools	Price	Description
Exar	Flexar Beta Family	Tile Array	26V	0.5 (npn) 0.012 (pnp)	30 analog	DOS-compatibles only	Flexar Integrated Design System	$6000 (Beta-66) $8500 (Beta-100) $12,500 (Beta-180) $18,500 (Beta-240)	The four arrays have 240, 180, 99, or 66 npn or pnp transistors (Beta-240, Beta-180, Beta-99, and Beta-66). Single-metal mask programs twinstor to be an npn or pnp transistor. Prices are for layout and integration.
Harris Semiconductor	HTA1000 and HDI1000	Tile array (HTA1000) standard cell (HDI1000)	40V	0.7 (npn) 0.4 (pnp)	26 analog (HDI1000)	HP/Apollo and Sun workstations	Fastrack, Cadence tools	$44,000 (HTA1000) $78,000 (HDI1000)	Library contains NiCr resistors, JFETs, zener capacitors, op amps, S/H circuits, mixers, and multipliers. Price is for 15 to 25 dc-tested package parts. Bipolar devices are dielectrically isolated.
	HTA2000 and HDI2000	Tile array (HTA2000) standard cell (HDI2000)	20V	1.2 (npn) 1.0 (pnp)	22 analog (HDI2000)	HP/Apollo and Sun workstation	Fastrack, Cadence tools	$44,000 (HTA2000) $78,000 (HDI2000)	Library contains NiCr resistors, JFETs, zener capacitors, op amps, S/H circuits, mixers, and multipliers. Price is for 15 to 25 dc-tested package parts. Bipolar devices are dielectrically isolated.
	HTA3000 and HDI3000	Tile array (HTA3000) standard cell (HDI3000)	10V	8.0 (npn) 4.0 (pnp)	26 analog (HDI3000)	HP/Apollo and Sun workstation	Fastrack, Cadence tools	$64,000 (HTA3000) $116,000 (HDT3000)	Library contains 100-MHz op amp, 400-MHz current-feedback amp, 50-MHz S/H circuit, and 300-MHz mixer. Price is for 15 to 25 dc-tested package parts. Bipolar devices are dielectrically isolated.
	HDI4000	Standard cell	80V 200V	0.3 (npn) 0.08 (pnp)	High-voltage amplifiers, high-voltage analog switches	HP/Apollo and Sun workstations	Fastrack, Cadence tools	$78,000	Bipolar devices are dielectrically isolated. Price is for 15 to 25 dc-tested package parts. Subscriber-line interface circuits (SLICs) in the library.
	HBC2500	Mixed-signal standard cell (optimized for analog)	5V, 16V	0.6 (npn)	51 digital 49 analog	HP/Apollo and Sun workstation	Fastrack, Cadence tools	$101,000	BiCMOS array has 3-μm effective gate length. Mixed-signal ASIC optimized for analog. Price is for 15 to 25 dc-tested package parts.
Interdesign	MM and MV family	Standard cell array	20V (MM) 40V (MV)	0.4 (npn) 0.003 (pnp)	23 analog, microcells	DOS compatibles (only)	Liberty OrCAD PSpice EXE-CLEAN	$25,000 MME version vendor designed $12,000 MME version customer designed	MM family has from 2 to 28 cell arrays separated by diffused resistors and cross-unders. MV family has monitors that function as lateral npn or pnp transistors. MME array has 12 cells, 90 npns, 46 pnps, 2 capacitors, 466 diffused resistors, and 9 pinch resistors.
NCR	VS700	CMOS standard cell	7V	NA	20 analog 180 digital	Sun and HP/Apollo workstation	Cadence, Viewlogic, and Mentor Graphics/ tools; Saber	$55,000 (25,000 gates) $70,000 (50,000 gates) $5000/wk (macro modifications)	Analog cells include comparators, DACs, ADCs, clock synthesizers, analog switches, general-purpose op amps, VCOs, and bandgap references.
Raytheon	RSC4000	Complementary BiCMOS standard cell array	13V	4 (npn) 1.5 (pnp)	27 analog cells, 37 digital cells	Sun workstation, DOS compatibles	OrCAD, Raytheon tools, Cadence tools, PSpice, HSpice	$40,000 to $60,000 (NRE)	Mixed-signal array has ECL and CMOS gates. Library contains amplifiers having 2 nV/$\sqrt{\text{Hz}}$ noise density, bandwidths beyond 200 MHz, slew rates key beyond 2000V/μsec, reference accuracy to 5%, and 1-mV offset voltages. CMOS logic operates from 3.3 or 5V.

tric trench to isolate the transistor from the rest of the array. Dielectric isolation is more effective than junction isolation, which electrically isolates transistors from one another using back-biased pn junctions. Dielectric-isolation transistors closely approximate off-the-shelf discrete transistors.

The HDI1000 and the HDI2000 standard cells have breakdown voltages of 40 and 20V, respectively. You can incorporate npn and pnp transistors, thin-film resistors, JFETs, capacitors, and buried zeners into 26 hard-coded macrocells. Hard-coded macrocells include op amps, comparators, S/H functions, voltage references, mixers, and multiplexers that have usable bandwidths as high as 60 MHz. The

Table 1—Representative analog-ASIC tile arrays (continued)

Company	Model	Family type	Breakdown voltage	Transistor f_t (GHz)	Macros	Design platforms	CAD tools	Price	Description
Raytheon	RPA160	Tile array	13V	4 (npn) 1.5 (pnp)	20 analog cells 50 digital gates	Sun workstation, DOS compatibles	OrCAD, Raytheon tools, Cadence tools, PSpice HSpice	$40,000 (NRE)	16 tiles in a 4×4 grid pattern. Each tile has 24 npn transistors, 18 pnp transistors, 2 Schottky diodes, 2 MOS capacitors, 13 thin-film resistors, 2 metal layers, and noise voltage density = 2 nV/$\sqrt{\text{Hz}}$.
	RLDA80	Macrocell array	32V	0.4 (npn) 0.4 (pnp)	8 analog gain cells, 54 digital cells	Sun workstation, DOS compatibles	OrCAD, Raytheon tools, Cadence tools, PSpice, HSpice	$30,000 (NRE)	40 npn transistors, 12 pnp transistors, 8 large resistors (100 to 200k), bandgap regulator for V_{DD}, V_{B1}, and V_{B2}, 128 thin-film resistors. Analog gain cells operate to 1 MHz. Two metal layers.
	RLA family	Cell array	32V	0.4 (npn) 0.004 (pnp)	8 complete analog gain cells, 7 partial analog gain cells	Sun workstation, DOS compatibles	OrCAD, Raytheon tools, PSpice, Cadence tools, HSpice	$30,000 (NRE)	Family comes with 4, 8, 12, or 16 macro cells. 49 npn transistors, 19 pnp transistors, 95 resistors.
Sipex	SP2000	Tile array	20V or 35V	1.0 (npn) 0.6 (pnp)	28 analog cells	DOS compatible, Sun workstations	PSpice, GDSII database	$18,000 (4-tile) $35,000 (20-tile) (NRE)	Family of five tile arrays having 4, 8, 12, 16, and 20 tiles. Total transistors are 180, 320, 484, 616, and 780, respectively. Large trimmable NiCr or SiCr resistors. Dielectric isolation. SP2107 has 390 npn transistors, 380 pnp transistors, 96 diodes, 48 capacitors, and 30 pinch resistors.
Tektronix	QuickChip 6	Tile array	8V	8.5 (npn) 0.08 (pnp)	15 analog cells	DEC and Sun workstations	PSpice, TEKSpice, QuicKic, Quick-Custom	$55,000	1, 4, or 12 symmetrical tiles contain 42 npn transistors, 25 pnp transistors, 12 Schottky diodes, 12 JFETs, 4 capacitors, and 300 resistors. Peripheral has large npn transistors and Schottky diodes for EDS protection. Two metal layers.
	QuickChip 7	Tile array	5V	12 (npn) 0.08 (pnp)	15 analog cells	DEC and Sun workstations	PSpice, TEKSpice, QuicKic, Quick-Custom	$55,000	Section optimized for digital ECL logic and separate analog section. Dielectric trench isolation. Four symmetrical macro tiles contain 208 npn transistors, 56 pnp transistors, 32 Schottky diodes, 24 capacitors, and 848 transistors.
	QuickTile	Custom tile array	8V	11 (npn) 0.08 (pnp)	15 analog cells	DEC and Sun workstations	PSpice, TEKSpice, QuicKic, Quick-Custom	$55,000	16 standard QuickChip, 6-tile arrays. Four combination QuickChip 6-tile arrays. You can rotate the tiles in 90° increments or mirror them around the x or y axis. Two metal layers.

HDI3000 standard cell has a breakdown voltage of 10V and usable bandwidths as high as 1 GHz. The HDI3000 uses two bonded wafers and dielectric trenches to achieve transistor isolation. The process, called UHF1, permits higher packing densities and a 5× to 10× speed improvement over the company's 20 and 40V devices.

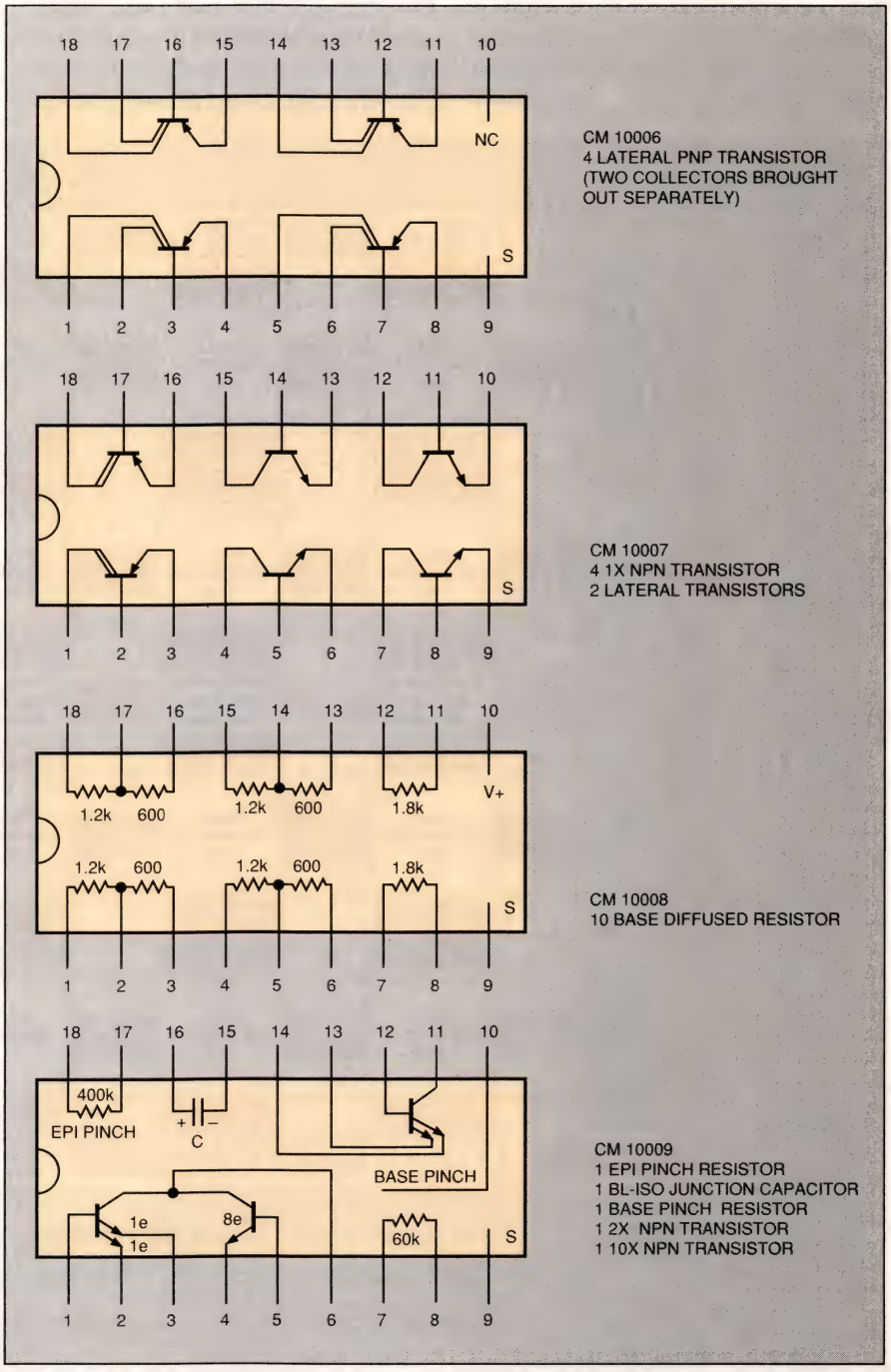
The Harris CAD tool, Analog Fastrack, was licensed to Cadence in 1990. Analog Fastrack is the basis for the Cadence Artist, a generic CAD tool that isn't limited to using the Harris process database. Analog Fastrack contains statistical models that let you vary one design parameter, while correlated parameters vary according to process equations. The CAD tools require an HP/Apollo or Sun workstation running Unix to design the analog ASIC and to run simulations.

Tile arrays get you down to basics

If you crave adventure or have simply decided that standard-cell macros won't get the job done, consider tile arrays. Tile arrays let you design at the transistor and passive-component level. Device-level analog ASIC design is not for the faint-hearted, however, no matter how experienced a discrete-level analog designer you are.

The reasons are many. Tolerances and temperature coefficients for on-chip components are much larger than their off-chip counterparts. In addition, you shouldn't expect the range of on-chip component values to be as large as off-chip parts, and on-chip inductors are virtually nonexistent. Bias voltages are another concern. Back-biased junctions used for isolation or on-chip capacitance should not be inadvertently forward biased by large signal levels. Some discrete configurations, such as composite npn and pnp transistors, may even oscillate when configured on chip because of the smaller parasitic capacitances.

Analog ASIC vendors create resistors using a variety of processes. Diffused resistors typically range from tenths of ohms to a few kilohms and have a resistor tolerance of ±25% and a temperature coefficient of 0.1%/°C. Pinch resistors use an epitaxial layer for resistance to achieve resistance value approaching 100 kΩ, but have 100% tolerances. Some vendors offer thin-film resistors that achieve 12% tolerances and temperature coefficients of 0.015%/°C. Thin-film NiCr resistors



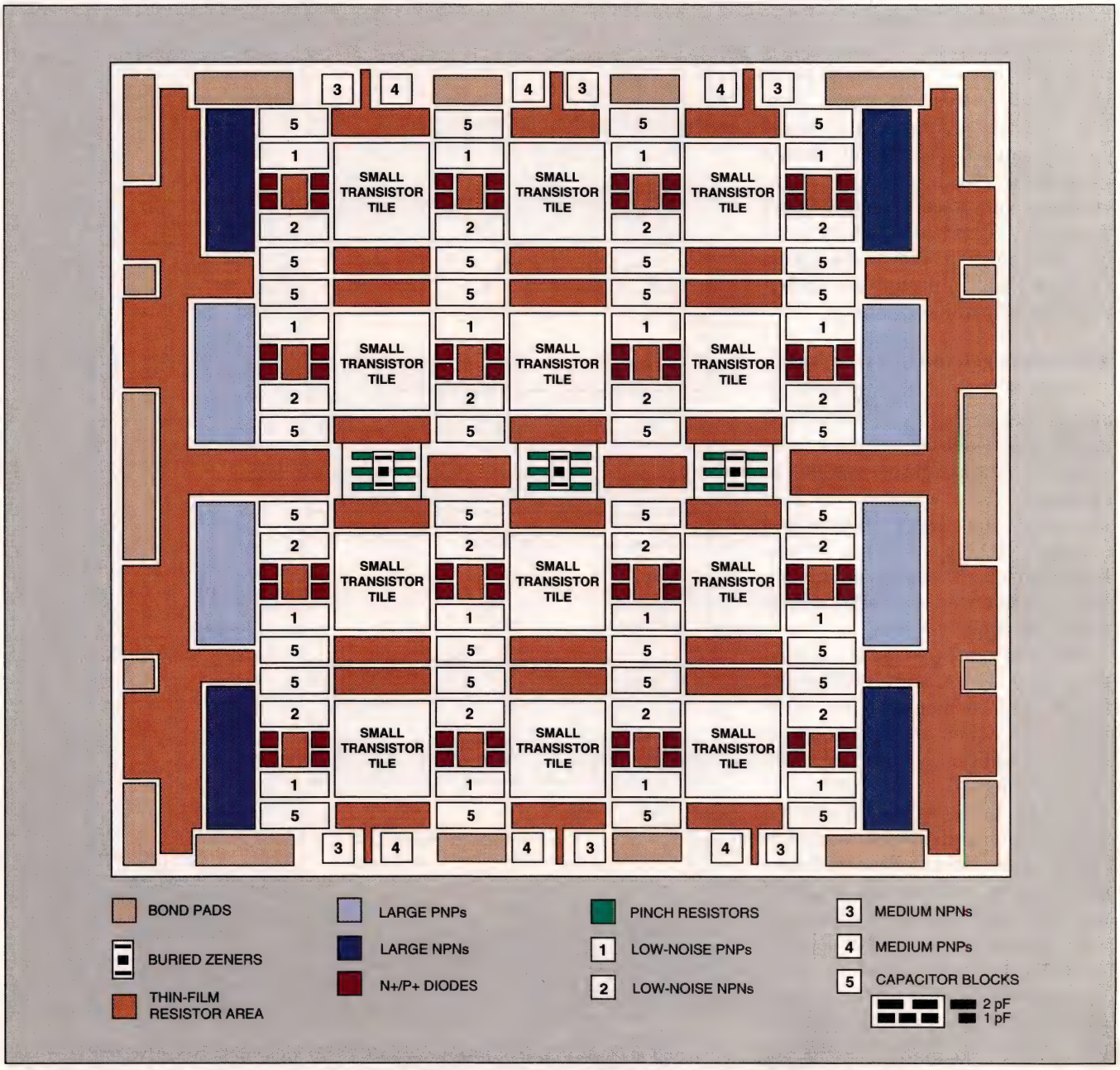
Analog kit parts let you breadboard a design before committing to silicon. These dual-in-line packages from Interdesign Custom Arrays Corp have discrete-level components that are representative of devices found on the MM and MV series of arrays.

Analog ASICs

have tighter tolerances than SiCr resistors, but have lower resistivity.

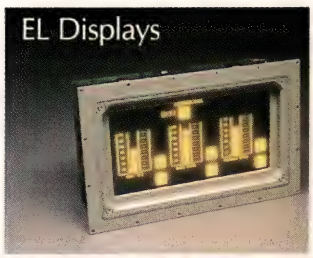
Analog ASIC vendors create capacitors using back-biased pn or MOS junctions. Capacitance values are 1 to 2 pF and tolerance values are ±10%. You can parallel these capacitors to achieve higher values, but the upper capacitance limit is probably 25 to 30 pF due to geometric constraints. Some vendors offer oxide capacitors, which can achieve higher capacitance values but lower dielectric resistances. With all these variations and limitations, what's a poor analog designer to do to achieve repeatable and consistent results?

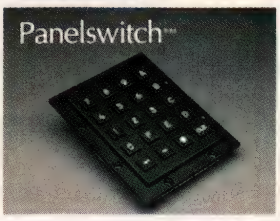
Fortunately, on-chip components have closer matching characteristics than off-chip parts and experienced chip designers use this attribute to accomplish design objectives. For example, two diffused resistors located close together on a wafer may differ from an absolute nominal value by as much as ±25%. However, the two resistor values may match each other by less than ±1%. Therefore, chip designers learn to design in terms of ratios. By using the ratio of the two resistors to configure a voltage divider or the gain of an amplifier, the nominal values cancel and the matching tolerances determine consistency.

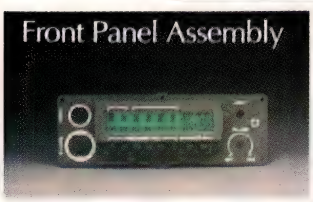


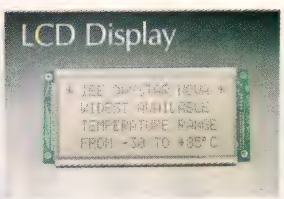
Tile arrays contain discrete-level transistors and components to create flexible semicustom designs. The SP2104 analog array has 12 small transistor tiles surrounded by a host of peripheral components.

Solid Building Blocks









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Circle #32 For Reference

Circle #33 For Immediate

You must also partition your design to fit the on-chip capabilities of the chosen tile array. Large resistor and capacitance values should remain off chip. Switched capacitor filters are more accurate than RC filters and all large inductors must be external to the ASIC. To make a long story short, there is no substitute for having an experienced analog ASIC designer watch over your shoulder to ensure that no ground rules are violated. All of the tile-array vendors provide consultant services where an experienced, vendor-supplied, chip designer inspects each level of the design task to ensure first-silicon success.

Arrays for nonconforming designs

If all of these warnings, forebodings, and cheap advice haven't scared you off, **Table 1** lists a number of tile arrays from which to choose. The dividing line between a standard cell and a tile array is gray, however. All of the tile arrays have macros to interconnect some predefined analog function. Interdesign Custom Arrays Corp, which emphasizes its large macro library for their MM and MV series of arrays, also includes a variety of discrete-level devices and microcells from which you can create custom standard cells. The dividing line is one of emphasis. Tile-array vendors generally expect design wins for analog designs that don't conform to standard macros. Therefore these vendors provide considerable flexibility in their arrays.

The QuickChip 6 and QuickChip 7 families from Tektronix are representative analog tile arrays. The QuickChip 6 family consists of three arrays having 1, 4, and 12 symmetrical analog tiles. (For a list of the descrete-level components in the QuickChip families, see **Table 1.**) Large npn transistors and four I/O drivers and large Schottky diodes for ESD protection surround the periphery of the wafer. The npn transistors have an f_t of 8.5 GHz and a collector-to-emitter breakdown voltage of 8V. Diffused resistors range from 250Ω to 4 kΩ and NiCr resistors are optionally available. **Ref 1** is a good example of a device-level low-noise amplifier design using the QuickChip 6 tile array.

The QuickChip 7 is twice as dense as the QuickChip 6 and contains four symmetrical analog tiles and a digital ECL section. The periphery of the chip contains 48 large npn transistors for I/O. The npn transistors have an f_t of 12 GHz and a col-

For more information . . .

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Analog ASICs

lector-to-emitter breakdown voltage of 5V. Both the QuickChip 6 and QuickChip 7 arrays have two layers of metal for interconnecting the blocks.

The QuickCustom start-up package includes a 2½-day training period at Tektronix to get familiar with the company's QuicKic design tools. Tektronix also assigns a product engineer to provide guidance through the design process, through prototype fabrication, and into production. Tektronix does not offer breadboard kits, however. Most of the other tile-array vendors offer a kit of SSI packages that contain representative transistors and passive components found in their arrays. With the exception of frequency response, which is affected by stray capacitance, a carefully constructed breadboard using kit parts can produce a representative circuit for evaluation.

Laser-trim resistors

The Sipex SP2000 family of analog tile arrays uses dielectric isolation for the vertical npn and pnp transistors in the array. The company fabricates the transistors in individual silicon islands that are surrounded by silicon dioxide. Sipex can laser trim the thin-film resistance area to achieve precise resistance values. Resistor temperature coefficients are as low as 0.01%/°C. The npn transistors have an f_t of 1 GHz and a collector-to-emitter breakdown voltage of 20 or 35V. The arrays have two metal layers for interconnecting the blocks. Kit parts of the discrete components and most of the 28 analog macros are available to evaluate designs before committing to silicon.

A unique feature of the Exar Flexar Beta family of arrays is the twinstor. Using the company's Flexar Integrated Design System on a DOS-compatible computer, you can program the twinstor to be an npn or pnp transistor using a single mask layer. This flexibility lets you mix and match any combination of bipolar devices on a single chip—even all npns or all pnps. Other tile arrays have dedicated areas on the chip for either npn or pnp transistors, which sometimes require long on-chip trace lengths to interconnect them. The twinstor lets you program npn or pnp transistors next to each other on the tile array.

As circuits shrink, pressure mounts on vendors to make analog ASIC design as easy as digital ASIC design. Surely large analog macro libraries are a step in the right direction. However, many of the quirks of analog design require special expertise. To achieve success in designing an analog ASIC, the customer must have a closer relationship with the analog ASIC vendor than needed with a digital ASIC vendor. Analog ASIC vendors are staffed with experienced analog designers to get you over the rough spots. EDN

Reference

1. "A Wideband Monolithic, Low-noise, Front-end Amplifier," Scott L Williams, Tektronix Technical Note.

Article Interest Quotient
(Circle One)
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HOW DO WE RATE?

During the past year, we've made some changes in EDN, and we'd like to know what you think about these enhancements. Please take a few minutes to look at our editorial questionnaire on pg 10.

The REMARKABLY DENSE ARGUMENT FOR THE CROSSPOINT FPGA.

10,000

useable gates on one 12K chip.

Field Programmable Gate Arrays have always been a promising sort of product. But they haven't had nearly enough useable gates. Not to mention their pitifully low performance. And as a

fig. 1
The Real World
It's a nasty, demanding place. Now there's an FPGA *with enough density to let you build the mainstream products that are used in it.*

result, the ASIC designer has seldom bothered with them. The Crosspoint FPGA is

EXHIBIT **A**
The product. In through-hole.

a dream product that breaks all this wide open. It offers up to 10,000 true, useable gates on one 12K chip, and it's fast. Will it change design permanently?

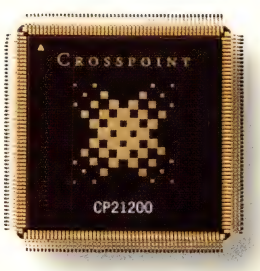

EXHIBIT **B**
The product. In surface mount.

We submit that it will.

In name, it's a 12K. But it gives you far more useable gates than that suggests. It's also fast. And predictable. All in all, a lot like a gate array. There's a reason.

IT *Is* A GATE ARRAY

Crosspoint gives you the industry's first 12K FPGA. But there's considerably more to it than that.

And, at the same time, less.

The Crosspoint FPGA offers unheard-of gate-utilization efficiency. The highest-available FPGA performance. And remarkable predictability with both.

All for one simple reason. Unlike *all other* FPGAs, Crosspoint's is—architecturally—a gate array.

Like a mask-programmable gate array, it has transistor-level granularity. And unlike previous FPGAs, it has gates.

Which, in itself, is noteworthy.

The smallest building blocks of all previous FPGAs are elaborate and complicated constructions—incorporating numerous logic macrocells with numerous functions. And resulting in an extremely complex chip for a rather modest number of "gates."

EXHIBIT **C**
Simplicity itself: our gate.

The smallest building block of the Crosspoint FPGA is something far simpler—a gate. A real one.

And that, in turn, is why our "12K" chip actually is a 12K—and gives you up to 10,000 useable gates—10,000 *true,* gate-array gates. Which is a gate-utilization efficiency of up to 85%. Efficiency comparable to that of other true gate arrays. And, of course, far in excess

of what you get from existing FPGAS.

Our superior *performance* is also due to our streamlined architecture. We function in systems with clock speeds up to 50 Mhz. Which may not seem altogether meaningful in the murky environment of FPGA performance claims. But is very meaningful when you consider that *other* FPGAS will only function in systems in the 15-30 Mhz range.

The *predictability* of the Crosspoint FPGA is significant in itself. As with a gate array, you'll know what size circuit you can fit on the chip, and what speed it will operate at. So you'll know you aren't just spinning your wheels.

And we also give you built-in testability logic, per the JTAG Boundary Scan Architecture Standard—which will make board testing painless, and assure high quality.

At a glance, that's what the product is — technically.

What it *means,* is that for the first time you've got the FPGA you need. One without limitations, that will let you use FPGAS where you'd like to. In real-world products.

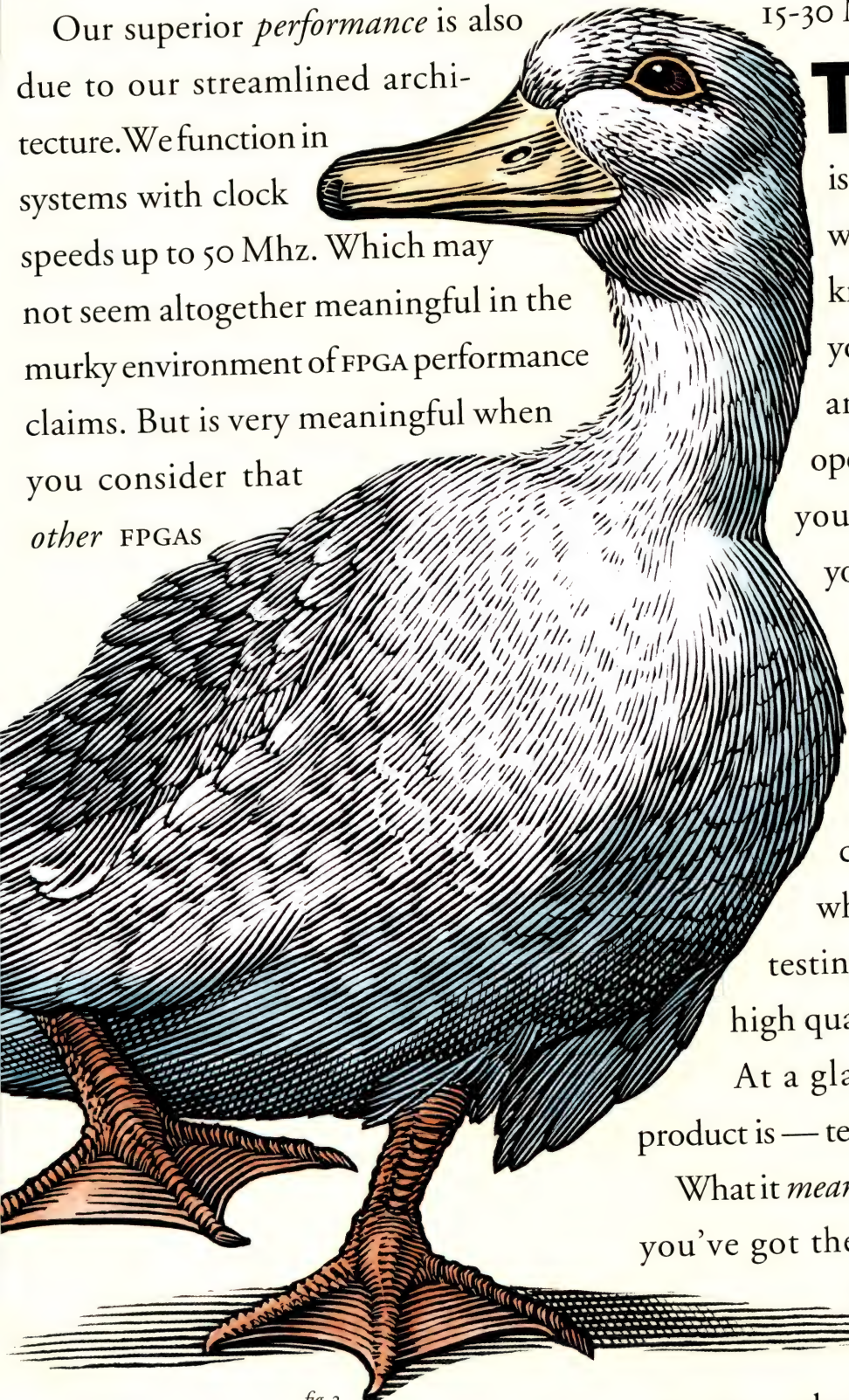

fig. 2
Duck
There's an old saying: If it looks like a duck, and acts like a duck, it must be a duck. Our FPGA *acts like a gate array, and is one.*

We'll also give you something else you can only get with a true gate array (and we think you'll especially appreciate our tools).

THE POWER *of* LOGIC SYNTHESIS.

Because of its gate array architecture, the Crosspoint FPGA is a perfect fit in the ASIC design environment.

It makes the cumbersome design methodology you associate with FPGAs, entirely a thing of the past.

For instance, Crosspoint's is the first FPGA that makes it viable to take advantage of logic synthesis, and use it to boost productivity.

The coarse granularity of previous FPGAs has made *using* logic synthesis so inefficient that there's been very little reason to do it. By contrast, the transistor-level granularity of the Crosspoint FPGA makes logic synthesis as efficient as it is with *any* ASIC.

Which is significant, because the extremely high useable-gate count that Crosspoint offers means there are big gains to be realized *with* logic synthesis.

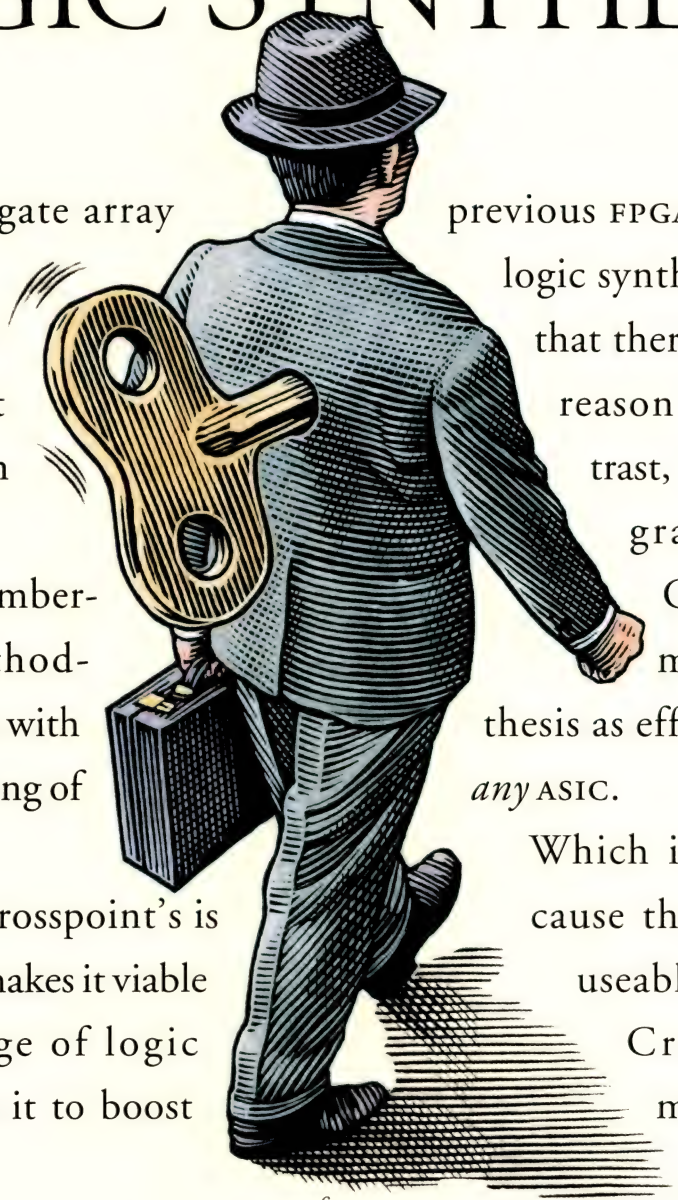

fig. 3

Your Own Automated Designer

You don't have to use logic synthesis, but there's a good reason to. Productivity. It's like having a clone of yourself. He excels at details and will go right where you point him.

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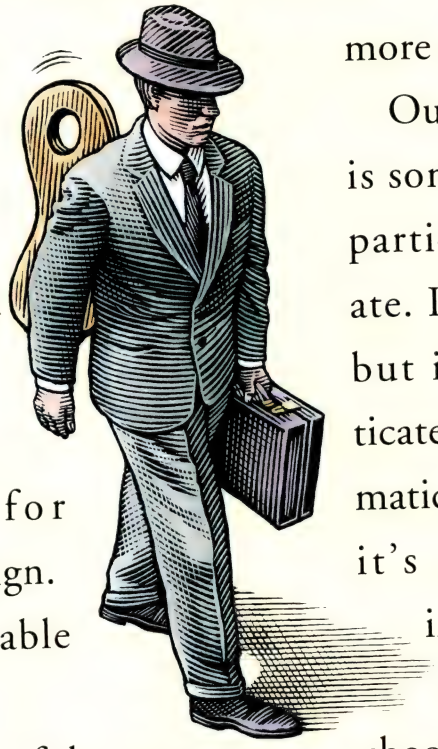


When it comes to the rest of design automation, you'll be able to use the tools you're familiar with. In precisely the ways you use them for standard ASIC design. And with predictable results.

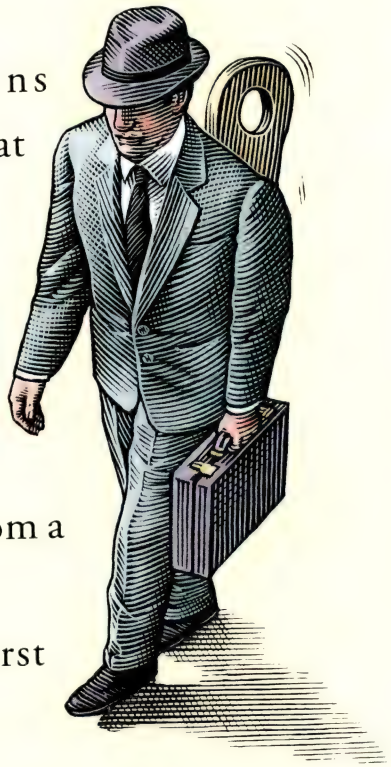
It is, in fact, one of the most important advantages we offer.

You'll find you can do both pre- and post-layout simulation. You'll have the familiar and efficient back-annotation path you expect with a gate array—something that's never previously been available for an FPGA.

And that will be true for any leading simulation product you work with. Crosspoint's Design Kits support the simulation, logic synthesis, schematic capture, and timing- and fault-analysis products of Mentor Graphics, Synopsys, Cadence/Verilog, Viewlogic. And more soon.

Our place & route is something you'll particulary appreciate. It not only *works,* but it's highly sophisticated. It's powerful, it's automatic, it's flexible, it's timing-driven, it's intuitive. And it offers an interactive editing capability that will help you fine-tune, if you choose to.

All in all, we've been careful to give you the tools that will make it not only feasible, but *easy* to realize the major gains that the Crosspoint FPGA allows for.



But those gains themselves are what matter most.

The sorts of density, performance, predictability—in fact *everything*—that you expect from a gate array.

Now, for the first time, in an FPGA.

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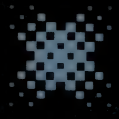

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EDITORS' EDN CHOICE

Vector signal analyzer brings amplitude and phase measurements to RF

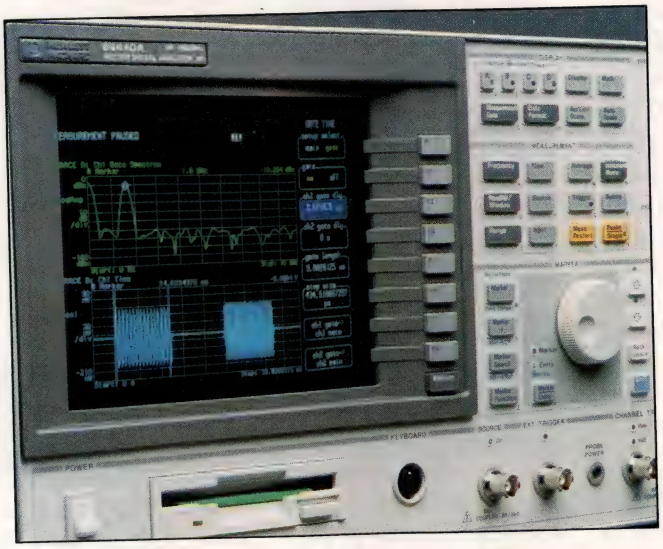
The increasingly complex RF signals being used in digital communication, medical and industrial ultrasound, and HDTV (high-definition TV) require test equipment that goes beyond traditional swept spectrum analyzers. You need to see more than just the amplitude of a continuous signal; you need to be able to analyze burst, transient, and vector-modulated signals.

"Vector signal analyzer" is the name invented by Hewlett-Packard to describe an instrument that accepts time-domain data and provides both amplitude and phase information in the frequency domain. It also offers a variety of demodulation and transient-analysis capabilities.

The HP 89410A ($28,500) vector signal analyzer covers dc to 10 MHz and provides one or two channels. The HP 89440A ($51,500) is an identical box with the addition of an RF section that translates one of the 10-MHz baseband channels to as much as 1800 MHz. You can use the HP 89411A ($9000) 21.4-MHz IF downconverter to provide narrowband analysis above 1800 MHz. Each analyzer converts the input signal to 25.6 MHz and uses digital signal processing to do the rest.

You can trigger on a burst or transient signal, store the data, and then set markers for analysis. By placing markers in the time domain, you can freeze a signal and then analyze only the sections you are interested in. You can then view the data in the frequency domain as amplitude and phase. You can also demodulate amplitude-, phase-, and frequency-modulated signals and display the data in the time domain.

For example, you can plot amplitude, phase, and frequency data vs time and easily see variations over time. Then you can convert this data into the frequency domain and get a spectrum of the demodulated signal.



The color display on the vector signal analyzer allows you to view multiple domains at the same time. You can move your markers in the time domain to select the portion of the signal you wish to analyze. At the same time you can see the spectrum of the signal within your markers.

This operation would be useful if you were designing a transmitter whose phase must be stable within a certain percentage before you can start sending data. You could sample the transmitter turning on in the time domain. Then you could surround the transient signal with markers and convert it to a plot of phase vs time. This plot would show the phase variation over time. You could then characterize the design to see how much you have to delay data transmission after the transmitter begins transmitting.

You can also trigger on the IF. This capability allows you to trigger on a signal in the frequency band of interest and adds frequency to your trigger options. If you are trying to analyze a burst signal within a broadband signal, you can set up the instrument to see only the frequency band where the burst exists, ignoring all other signals.

The analyzer has a number of other functions, like correlation, coherence, and cross-correlation, usually found on an FFT type of spectrum analyzer. The front-panel-mounted disk drive can store setup data, acquired signals, or programs, and can also be used to perform field updates of the instrument's software, which is stored in EEPROM. Waterfall and spectrogram displays are optional. Another option is the vendor's Instrument Basic programming language. A PC-compatible keyboard plugs in for program development, and an IEEE-488 interface is included. Delivery is eight weeks ARO.—**David Shear**

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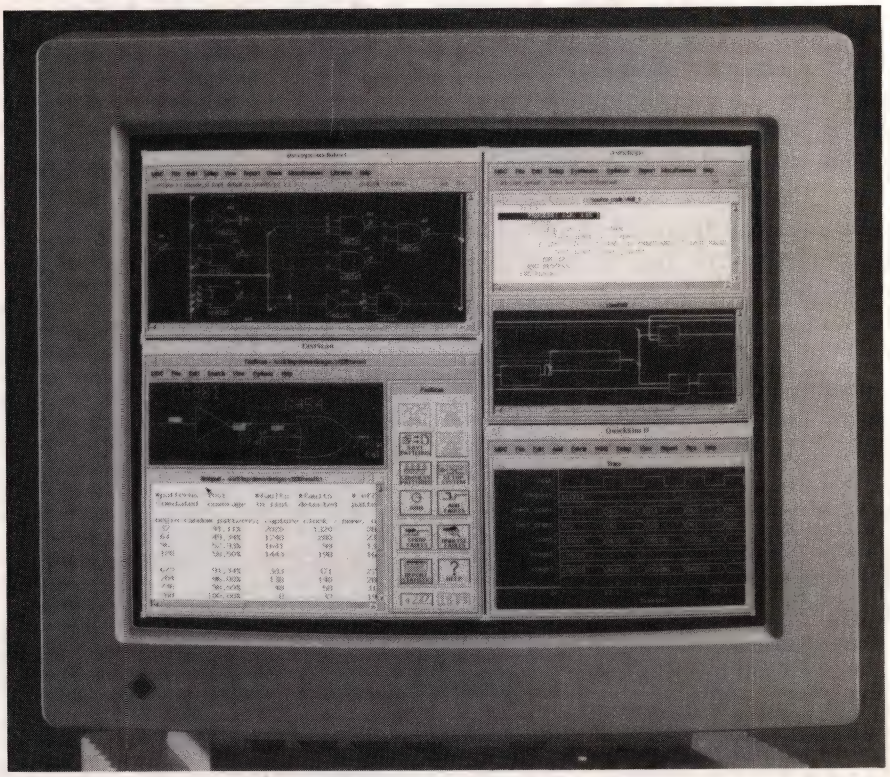
Circle No. 383

Tool set joins synthesis with simulation for reliable ASIC design

Right-first-time silicon, the Holy Grail of the EDA (electronic-design-automation) industry, is being sought and found on routine designs. But, below 1-μm-feature size and above 60,000 gates or a 33-MHz clock rate, advanced ASIC designs tend to frustrate the quest for predictability. The more complex tools required for such designs often operate at cross purposes with each other—in particular, the synthesis and simulation features of advanced-design tool sets that rely on successive estimations, approximations, and generalizations. Recently developed tools also let users specify constraints and rules for the tools to use, increasing the probability of conflict between the assumptions that various tools make about your design.



The Top Down Design-Solver integrates VHDL-based design from concept to production and includes multilevel design capture, logic synthesis, logic simulation, VHDL simulation, and several test tools.

The Top Down Design-Solver is Mentor Graphics' answer to the quest for predictability in advanced designs. Described as a "top-down design system," the product strives for maximum accuracy in synthesis and simulation across its six tool groups. The tool set includes Design Architect for design creation, Quicksim II for functional verification, Autologic for synthesis, Quickpath for timing analysis, Flextest/Fastscan for design-for-test, and Quickcheck for design rule checks.

The tool set maintains consistency between hardware description language (HDL), resistor-transistor logic (RTL), and gate-level descriptions of a design by avoiding redundancy across multiple tools. Tools share data and functions wherever possible and have consistent timing models. The software uses a single ASIC library, one timing calculator, one VHDL (VHSIC-hardware-description-language) compiler for both synthesis and simulation, one simulator for both behavioral and gate-level work, and a common database for all tools.

Five ASIC and FPGA (field-programmable-gate-array) vendors (Fujitsu, LSI Logic, Mitsubishi, VLSI Technology, and Xilinx) will deliver design kits during the fourth quarter of 1992 for both Sun and HP versions of the tool set. The libraries will cover technologies that account for more than 80% of new design starts from these vendors. Mentor expects design-kit support by the end of 1992 from a total of 35 vendors representing more than 125 technologies.

Design centers that deliver support services to users of the tool kit have opened in San Jose, Denver, Dallas, Boston, Munich, and Tokyo. A program called Smartstart that includes Mentor, Sun Microsystems, and ASIC vendors delivers endorsements of design flows and individual customer support for software, hardware, and silicon fabrication. Users of the tool kit have produced at least six ASICs to date. Design-Solver is available immediately for Sun SPARCstations and HP 400 and 700 series workstations. Prices start at $135,000.

—John C Napier

Mentor Graphics Corp, 8005 SW Boeckman Rd, Wilsonville, OR 97070. Phone (503) 685-7000.

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CIRCLE NO. 57

Firmly entrenched in everything from your morning-coffee machine to the elevator in your building to massively parallel supercomputers, μPs and μCs have nowhere to go but up. (Photo courtesy Motorola Inc; concept, Staats Falkenberg & Partners Inc; photography, Tomás Pantin)

EDN's 19th Annual µP/µC Chip Directory

Providing at-a-glance performance and architectural data, EDN's revamped µP/µC directory details the key design info for 43 chips.

Ray Weiss, Technical Editor, and Julie Anne Schofield, Senior Associate Editor

This is a designers' directory, aimed at giving engineers the hard data they need to survey the microprocessor/microcontroller (µP/µC) field and get a feel for which chip to use. The directory includes 43 entries, ranging from low-end 8-bit 6502/6500s to high-end RISC processors like the 32-bit superscalar SPARCs or 64-bit superpipelining Mips R4000. All of the chips are in production or sampling, and each receives a full page of detailed description.

Design times have changed, and EDN's Microprocessor Directory, begun in 1973, has changed as well. This year's directory features up-to-date formats and a design-oriented approach. We have rewritten the directory from scratch, targeting design-ins for this fast-moving decade. We have dropped a number of old favorites, chips with outstanding design records such as the 8048 and the 6800, to make room for the new processors engineers will be designing in.

Microprocessor-based design has come of age. When EDN first introduced this directory, µPs were new and unknown components. Engineers then needed to get up to speed and learn how

to design-in μPs, substituting processor power for logic and electromechanical power. Today's engineers are different. Many of you cut your design teeth on μPs—it's not a new technology to you. And most of you have your favorites, architectures that you've relied on for years. Yet today's fast product turnarounds and critical cost demands are forcing many to expand their μP base, selecting the best, most cost-effective chip for each design project.

Exploring the possibilities

The new EDN directory format provides an overview of all mainstream μPs and μCs. You can use this as a resource, a base to view the available chips as combinations of price, power, and peripherals. This directory combines an architectural top-down approach with a bottom-up listing of processor features and performance numbers. You get a thumbnail overview, which characterizes the processors, coupled with real-world numbers pegging processor performance, power, and packaging.

Each entry page includes a quick-read table in the upper right-hand corner for a fast review of each chip's capabilities. This table consists of two side-by-side bulleted lists. The left list details the key functional chip parameters (number of registers, amount of RAM/ROM/cache(s), bus characteristics, etc), and the right list details the key performance numbers (clock rates, ADD times, MPY times, memory read/write cycles, maximum interrupt latency, etc).

Manufacturers of μCs and μPs

For more information on μCs and μPs such as those described in this directory, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Analog Devices
Literature Center
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Dallas Semiconductor
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Dallas, TX 75244
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FAX (214) 450-0470
Circle No. 308

Echelon
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Palo Alto, CA 94304
(800) 258-4566
FAX (415) 856-6153
Circle No. 309

For Echelon's Neuron chip:
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The directory covers chips in two categories: μCs and μPs. Microcontrollers are single-chip μPs that are basically self contained—they have on-chip resources, such as RAM and ROM, so they can stand alone. (They can access external, off-chip memory, however.) Microprocessors need external memory to run, microcontrollers do not.

Sizing the μP/μC

There has always been some confusion in assigning bit sizes to μPs and μCs. To some engineers, a processor's external bus width defines its base CPU size. A classic example is the 8088, a 16-bit CPU with an 8-bit external bus. Many classify it as an 8-bit machine. Of course, this approach can have a few problems. Not the least of these is what do you do with a microcontroller like Motorola's 68HC05 or Microchip's PIC 16Cxx, that has no external bus? Do we call it a "zero-bit processor?"

This directory takes a different tack for assigning processor sizes. We've evaluated processor sizing characteristics in a priority order, starting with ALU width, followed by register size, data path width, instruction word, and external bus widths. For example, a Siemens 80C166 having a 16-bit ALU, 16-bit registers, 16-bit instructions, 32-bit instruction (2-word) path, and an 8- or 16-bit external bus is defined as a 16-bit machine. So is a Motorola 68HC16 with 16-bit ALU, registers, and instructions, and an 8- or 16-bit bus. Our old friend the 8088, with its 16-bit ALU,

Motorola Inc
6501 William Cannon Dr W
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Jim Reinhart (68000)
Gary Montgomery (88000)
Rosemary Stone (RISC chips)
Lisa Hemple (μCs, DSP chips)
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(714) 975-8522
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From nsec to MHz and back again

Many of the entries in this directory mix clock rates and time specs in detailing CPU performance. Some performance numbers, such as for an ADD, may be given in clocks rather than nsec. With a clock-based performance measure, you can choose a clock speed and see the performance at that rate.

I don't know about you, but I've always had trouble converting back and forth between MHz clock rates and nsec periods. That is, until I stumbled onto the "lazy man's way" of conversion. It's simple: just take any frequency, say 20 MHz, and multiply it by the number needed to equal 1000 as a product. The number you just plugged in is the clock period in nsec. This method works both ways: for estimating the clock period, given its frequency, and for estimating the clock frequency, given its period. Here is the 20-MHz example:

$$20\ \text{MHz} \times X\ \text{nsec} = 1000,$$

so X = 50 nsec—period of 20-MHz clock. Similarly,

$$Y\ \text{MHz} \times 100\ \text{nsec} = 1000,$$

so Y = 10 MHz—clock rate for 100-nsec period.

This is an easy approach (except for odd numbers like 69 MHz). It's easier because many of us are better at guesstimating numbers than we are at dividing. Here's how it works:

$$f = 1/T,$$

where f is frequency, T is period, and fT = 1.

Remember in engineering school all the emphasis our professors placed on units and unit scales? Well, if you plug in MHz (10^6) and nsec (10^{-9}) it all falls out nicely:

$$\text{if } fT = 1,$$
$$\text{then } (M \times 10^6) \times (N \times 10^{-9}) = 1,$$

where M × N = 1000, M = frequency in MHz, and N = period in nsec.

Using this directory

Top view

Overview: Gives a brief glimpse of each chip or chip family.

Vendors/pricing: Lists the chip vendors and some representative pricing. In general, we list second sources but do not give second-source pricing. The idea is to give you an idea of general pricing and leave it to you to find the best price/service/delivery combination. Prices are per 10,000 units unless otherwise noted.

μP/μC characteristics: Bullet items list the key features (left column) of each chip or chip family. This includes basic architectural details such as number of registers, structure, external bus, address space, RAM and ROM sizes, peripherals, I/O pins, and number of external interrupts. RAM and ROM is on chip unless otherwise specified.

μP/μC performance: Bullet items list the key performance parameters (right column) for a chip or chip family. These parameters include ADD, MPY, and DIV times; external bus read/write cycle times; maximum interrupt latency.

The performance specs are generally for the top clock rate listed. Performance may be for one specific chip, which will be listed. Many ratings will be given in clocks, which can be converted to time after selecting a clock rate.

In both bullet lists, slashes mean "or" and commas mean "and." For example, "12/16-MHz" clock means that chip versions have a 12- or 16-MHz clock. And "8-kbyte data, instr caches" means that the chip has an 8-kbyte data cache and an 8-kbyte instruction cache.

Architecture

Architecture: A detailed explanation of each chip architecture, which touches on the key features. If there is enough room, it may include mini-summaries of operational characteristics such as addressing modes and special instructions.

Block diagram: A block diagram of a representative chip or the generalized design. The diagram is generic or labeled as a specific chip.

Variations\peripherals\interfaces: A catchall subsection that generally lists chip variations for μPs or μCs, key peripherals for μCs, or key interfaces for a chip.

Support

Hardware support: Lists chip features for testing and debugging code, hardware tools such as ICEs (in-circuit emulators) and logic analyzers, and evaluation boards. Generally does not list individual hardware vendors. You can get that information from the chip vendor.

Software support: Lists software tools and operating software available for the chip or chip family. Mentions languages available and some special software. Generally doesn't list individual software vendors. You can get the contact information from the individual chip makers.

Table 1—Index to μP and μC chips in EDN's annual directory

ALU width	Page	μC/μP
8 bits	81	Echelon Neuron
	82	Intel 8051/8052
	86	Microchip PIC 16Cxx/17Cxx
	90	Motorola 68HC05
	91	Motorola 68HC11
	92	National Semiconductor COP8
	94	NEC 78K
	95	Rockwell/WDC 6502/6500
	97	SGS-Thomson ST6
	98	SGS-Thomson ST9
	99	Texas Instruments TMS370
	100	Toshiba TLCS-90
	102	Zilog Z8
	103	Zilog Z80
16 bits	104	Hitachi H8/300/500
	108	Intel 8086/80186
	113	Intel MCS-96
	114	Mitsubishi 37700
	115	Motorola 68000
	116	Motorola 68HC16
	119	National Semiconductor HPC
	120	Oki 65/66/67K
	121	Siemens 80C166/167
	122	Togai FC110
32 bits	127	AMD 29000
	128	ARM VY86Cxxx
	129	AT&T Hobbit
	132	Cypress hyperSPARC
	135	Fujitsu SPARClite
	136	Hewlett-Packard PA RISC
	139	Hyperstone E1
	140	Intel 80386/80486
	143	Intel i860
	144	Intel i960
	147	Mips R3000
	148	Motorola 680x0
	151	Motorola 683xx
	152	Motorola 88K
	155	SGS-Thomson Transputer
	156	SPARC
	157	Texas Instruments TMS340
	158	Texas Instruments SuperSPARC
64 bits	161	Mips R4000

registers, and data path, and 8-bit bus is also tagged as a 16-bit μP.

Some processors bridge the gap between different data-word bit sizes. For example, you can address and use the 80386's general-purpose registers as 8-bit registers; and the Mips R4000 has a 64-bit ALU and registers, but supports 32-bit register addressing and arithmetic. The Hitachi H8/300 has 16-bit registers and ALU, but supports 8-bit registers and arithmetic.

Comes the revolution

The 1990s design world is driven by an accelerating microprocessor revolution. This is no longer a "doing business as usual" world, but rather a world in revolution, undergoing a changeover comparable only to the electrification of America in the late 1800s. And this revolution is changing the quality and texture of modern life and business, as well as engineering.

Microprocessors are now everywhere: running blenders and toasters, monitoring and managing buildings, controlling car engines and displays, and managing phones. They also are embedded in packaged applications such as smart car keys and toys. There are two evolutionary microprocessor-based design waves. First, the current microprocessor wave builds on microcontrollers—complete fixed solutions with program and peripherals dropped into place. The second wave, now forming, brings more flexibility with distributed control and reloadable intelligence.

References

1. Slater, Michael, ed, *Microprocessor Report*, $445/year, 874 Gravenstein Hwy, Suite 14, Sebastopol, CA 95472, (707) 823-4004, FAX (707) 823-0504. This triweekly newsletter is an excellent source for tracking μPs and μCs.

2. Johnson, Mike, *Superscalar Microprocessor Design*, Prentice-Hall Inc, Englewood Cliffs, NJ, 1991. The only technical book to explore in detail superscalar processor design. Good analysis and set of definitions.

3. Ganssle, Jack G, *The Art of Programming Embedded Systems*, Academic Press Inc, San Diego, CA, 1992. Well-written book explores embedded-system design and programming.

4. Hintz, Kenneth J, and Daniel Tabak, *Microcontrollers—Architecture, Implementation, Programming*, McGraw Hill, New York, 1992.

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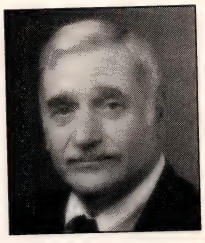

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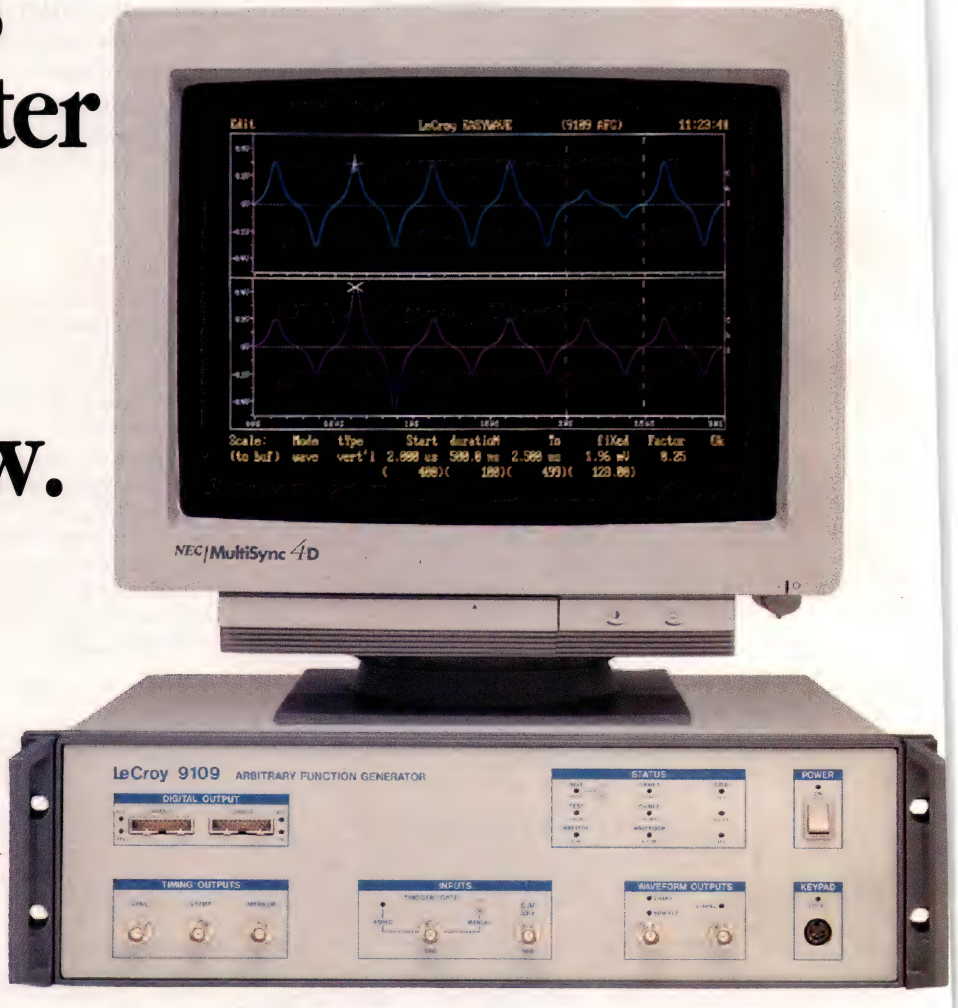

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OUTPUT LEVEL	10V p-p (50Ω)	10V p-p (50Ω)	10V p-p (50Ω)
DIGITAL PATTERNS	No	Yes	Yes

LeCroy

Innovators in Instrumentation

CIRCLE NO. 39

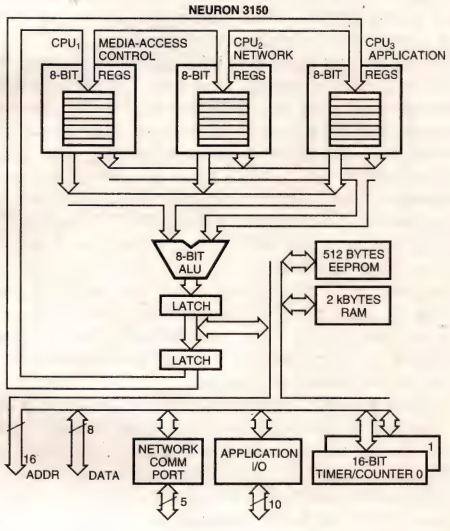
☐ **OVERVIEW** Echelon isn't a chip vendor. Instead, the company supplies network systems—microprocessors, transceivers, boards, software, development tools, and the Lontalk network protocol—for industrial/commercial control and building automation. In 1990, Echelon announced the 8-bit Neuron chips as the base for these networks. The chips' innovative design suits network control, and Echelon engineers created an extended version of C—Neuron C—that simplifies network control. Toshiba and Motorola build Neuron chips for general sales. The family comprises two chips: the 3150 and the 3120. The 3150 has 2 kbytes of RAM, no ROM, 512 bytes of EPROM, and runs out of memory. The 3120 has 1 kbyte of RAM, 10 kbytes of ROM, 512 bytes of EEPROM, but no external bus.

☐ **VENDORS/PRICING** Toshiba: TMPN3150, $10; TMPN3120, $10. Motorola: MC143150FU (64-pin QFP), $9.31; MC143120DW (32-pin SOG) sampling, $9.31.

Echelon Neuron

- 3 shared, pipelined CPUs with common memory, ALU
- Stack architecture; each CPU has 6 regs for status, addressing RAM
- 74 instr
- 10 kbytes ROM (3120)
- 512 bytes EEPROM (3120); 512 bytes EPROM (3150)
- 1 kbyte RAM (3120); 2 kbytes RAM (3150)
- Ext bus (3150): 16-bit addr, 8-bit data
- 2 16-bit timer/counters, 3 watchdog timers
- Network transceiver port
- No intr; 11 I/O pins
- 0.625- to 10-MHz ext clock; divide-by-2 internal
- 1.8-μsec mem-to-reg ADD
- 0.6-μsec NOP
- No MPY, DIV
- 2-clock ext R/W (200-nsec cycle)
- 16.7-kbyte/sec DMA I/O; 1.25-Mbps DMA network, 255-byte max transfer size
- PWM: 8 bits at 19.5 kHz
- 0.2- to 25.6-μsec timer/counter resolution

ARCHITECTURE



Echelon's 8-bit Neuron chips represent a new tactic in application-specific processors. Echelon engineers broke network control at a node into three areas: media-access control, network-protocol processing, and application processing. Instead of having these task groups time-share a single CPU, the designers dedicated a CPU to each group to eliminate task-switching overhead. Thus, each Neuron chip has 3 CPUs, which share on-chip resources such as RAM, ROM, EEPROM, the ALU, and chip peripherals. The chips have no interrupts; each CPU simply polls the peripherals and status words for events.

Each CPU has a 3-stage pipeline, which simplifies resource sharing between CPUs. Each pipelined CPU executes at a different pipeline stage, so all three can execute concurrently. As processing continues, the CPUs advance through all the stages for each instruction.

The CPUs are stack oriented. Each has a dedicated stack space in its 256-byte page in RAM. Stack-managing CPU registers include a 16-bit next-instruction pointer; a 16-bit base page pointer; an 8-bit data stack pointer that references data in the base page; a return stack pointer that addresses a call-return stack in the base page; and a top-of-stack register pointer.

Most instructions take 1 to 7 CPU cycles, or 0.6 to 4.2 μsec with a 10-MHz external or 5-MHz internal clock. A short branch takes 1 cycle, or 600 nsec; a far branch takes 4 cycles, or 2400 nsec. Operations push or pop data and registers on or off the stack. The top of the stack can be incremented or decremented. Most programmers, however, won't see these details because they'll be programming in Neuron C, an extended version of C for Neuron chips that builds in node-to-node communications.

Lontalk network protocol—7-layer protocol matches the OSI stack. Defines data-packet rates up to 1.25 Mbps; 700 packets/sec peak, 560 packets/sec sustained. Message-authentication service on network; 3-level addressing structure (domain, subnet, node) with up to 32k nodes/domain.

Network variables—Data items in protocol (single item or array) declared in application and available over network. Changes automatically propagate through network.

Lontalk message services—4 types: end-to-end acknowledged (most reliable); request and response; unacknowledged repeated; and unacknowledged (least reliable).

☐ PERIPHERALS

EEPROM—Holds 48-bit ID for each chip and network configuration. Can also hold application code or data.

I/O pins—Programmable I/O pull-ups; can sink 20 mA.

Timer/counters—Two 16-bit timers with selected I/O-pin input. Can configure for frequency or 1-shot output, pulse counting, input- or period-time measurement, quadrature input-edge counting (gray-code conversion), and input-edge counter.

Transceiver—In single-ended mode, interfaces to active transceivers for RF, IR, fiber-optic and coaxial-cable communication using differential Manchester encoding/decoding. In differential mode, drives/senses twisted-pair transmission line. Special-purpose mode for using power lines themselves as a transmission medium.

Host CPU interface—8-bit (3-bit control) bidirectional interface for external processor; can be configured as master or slave.

Serial I/O—Adjacent I/O pins can be serial-I/O- and clock-line pair. Also, 3-wire Neurowire or asynchronous serial port can link Neuron chips.

On-chip ROM (3120)—Holds Lontalk protocol code, event-driven task scheduler, application function libraries. Data and code in off-chip ROM for 3150.

External memory (3150)—16,384 bytes reserved for Lontalk; 43,008 bytes left for application code and data. Direct interface to off-chip memory, no glue logic required.

Neuron 3120/3150

Mode	Current (max)	Voltage (V)	Clock (MHz)
Normal	35 mA	5	10
Sleep	2 mA	5	10

3150 in 64-pin QFP; 3120 in 32-pin SOIC.

SUPPORT

☐ **HARDWARE** Hardware tools include a high-end Development Station box that requires a PC for the front end. The box holds multiple nodes, with or without emulator capability, and also serves as network monitor and protocol analyzer. Echelon sells node boards, network-router boards for linking subnets, and transceiver boards for different media. Third parties are also starting to provide boards. To defray hardware-tool cost, Echelon has a lease/rent program, as well as a test-drive program.

☐ **SOFTWARE** Echelon software tools range from a dedicated C compiler (for Neuron C) to network-management and hardware/software-debugging tools, including source-code-emulation debuggers. The compiler builds network variables into application code. These variables are actually network messages that are limited to 31 bytes. A change to a network variable results in the new value being distributed to interested network nodes. Also available is an application program interface for DOS and Windows control programs.

☐ **OVERVIEW** Many designers view the 8051/52 as the "Model T" of 8-bit μCs. Intel introduced the 12-MHz 8051 in 1980. Since then the chip has proliferated with a wide range of clock speeds and peripheral mixes available from Intel and second-source vendors. Contributing to the 8051/52's popularity is its large base of development tools. Clock rates have reached 40 MHz. For further speed-ups, vendors are working on faster 8051/52 cores.

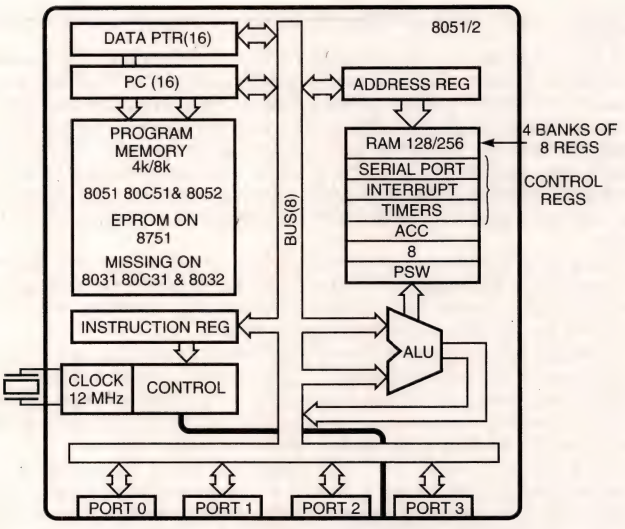
☐ **VENDORS/PRICING** Intel has licensed the 8051 to several vendors including AMD, Dallas Semiconductor, Philips/Signetics, Matra, and Siemens. Both Philips/Signetics and Siemens have been especially aggressive in extending the 8051 with specialized peripherals and versions. Oki has redesigned the 8051 core for its nX 65K/66K/67K μCs.

Intel 12-MHz 87C51GB, $19.80; 87C51, $11.50. Oki 12-MHz 83C154, $4.49; Signetics 33-MHz 80C51, $3.50.

Intel 8051/52

- Accumulator-based CPU
- Sets of 4 banks of 8-bit registers in RAM
- 46 instr
- 64/128/256 bytes RAM
- 2 to 32 kbytes ROM/EPROM
- Direct, indirect addressing (both restrictive)
- 2 64-kbyte address spaces for instr, data; can combine spaces off chip
- 2 16-bit timers
- 2 ext intr min
- ADC with later versions
- 12/16/20/24/30/33/40-MHz clock
- 12 clocks=1 cycle=1 μsec at 12 MHz
- 1-cycle NOP; 2-cycle ADD-to-A, MOVE-to-A
- 2-cycle JUMP, CALL/RET
- 4-cycle MPY, DIV
- No penalty for ext code access; ext access must be indirect for data
- 9-cycle max intr latency

ARCHITECTURE



The 8051 is both a register- and accumulator-based design. The CPU has 4 banks of eight 8-bit registers in on-chip RAM. On-chip RAM also holds addressable memory and special-function registers that define peripheral operation and configurations. Most data-manipulation and memory-load instructions go though the A register accumulator.

Trying to live within an 8-bit on-chip data-addressing budget, Intel designers overlapped data address spaces. The lower 128 bytes of RAM hold the registers, a bit-operation area, and a RAM area. These lower bytes can be addressed directly using an 8-bit value. The upper 128 bytes of on-chip data RAM encompass two overlapping address spaces. One is for directly addressed special-feature registers; the other for indirectly addressed RAM.

Register indirection uses an 8-bit register for an on-chip RAM address; an off-chip address needs a 16-bit pointer register (DPTR). The 8051/52 (except for Siemens μCs) has only one DPTR, which cannot be indexed. You can, however, increment the 16-bit DPTR.

The 8051 can use on- or off-chip memory for the two 64-kbyte instruction and data spaces. You can combine these spaces by ANDing pins together. The instruction and data spaces share an external bus, which comprises ports 0 and 2. For 16-bit operation, the bus is multiplexed and requires a buffer to hold an address stable while moving data.

The 8052 followed the 8051 and has increased RAM and ROM and more peripherals. Later versions added an ADC, programmed counter arrays (smart, general-purpose timer/counters with capture registers), serial channels, a multichip bus, and more external interrupts and I/O pins.

Siemens and Signetics have added more on-chip RAM, which they call X-memory. This memory is treated like external data memory and also requires indirect addressing. Siemens also extended the architecture by adding additional 16-bit pointers to make indirect addressing easier. The 8051/52 has two power-reduction modes: idle and power down.

Stack—8051 implements stack in on-chip RAM. CALL/RETs automatically push/pop PC.

Code constants—Algorithm constants can be stored in program space. Can move a byte from indirect-addressed program memory to accumulator using DPTR.

Jump ranges—Three ranges for jumps: ±128 for SJMP, within a 2-kbyte page for AJMP, and within a 64-kbyte range for long jumps. Similar limits exist for subroutine calls.

Increment/decrement—You can increment and decrement regs, accumulator, and DPTR for looping or indexing. Can also decrement a reg or byte in direct-access RAM and branch on results.

Bit operations—Bit set, bit clear, complement for a 16-byte area of RAM. Can AND or OR bits with carry bit.

μP	Mode	Max current at 5V	Clock (MHz)	Pins, package
Intel 87C51 (basic 8051)	Run	20 mA	20	40-pin DIP 44-pin QFP
	Idle	5 mA		
	Power down	50 μA	40	
Siemens 80C501	Run	55 mA		40-pin DIP 40-pin PLCC
	Idle	28 mA	12	
Signetics 83C751	Run	20 mA		24-pin DIP 28-pin PLCC
	Idle	5 mA		

VARIATIONS

Intel 87C51GB—8052 with 48 I/O pins, 2 programmable counter arrays, 8-channel ADC, three 16-bit timer/counters, watchdog timer, UART, PWM.

Intel 80C58—32 kbytes EPROM, 256 bytes RAM, 32 I/O pins, programmable counter array, three 16-bit timer/counters.

Dallas Semiconductor DS5002FP—Secure 8051, has built-in address and data encryption, 40-bit random-key encryption, watchdog timer, power monitor.

Matra 80C154—Runs to 30 MHz. Static design, has 16 kbytes ROM, 256 bytes RAM, 32 I/O pins. Draws 35 mA at 30 MHz, 5V.

Oki 83C154—Low-height 8052 for PCMCIA and disk controllers. 1.3-mm max height in thin, 44-pin QFP. Clock to 22 MHz.

Siemens SAB80C501—40-MHz 8052, has 8 kbytes ROM, 256 bytes RAM, three 16-bit timer/counters. Can run at 12 MHz, 3.3V for low power.

Siemens SAB80C517—8052 with 16-bit MPY/DIV unit, 4 timer/counters with capture/compare regs, 56 I/O pins, 8 data pointers, watchdog timer, ADC, 2 serial ports.

Signetics 83CL51—Low-power version, 1.8 to 6V, 32 kHz to 20 MHz, warm start, I^2C serial bus. Draws 2.5 mA at 3 MHz, 1.8V.

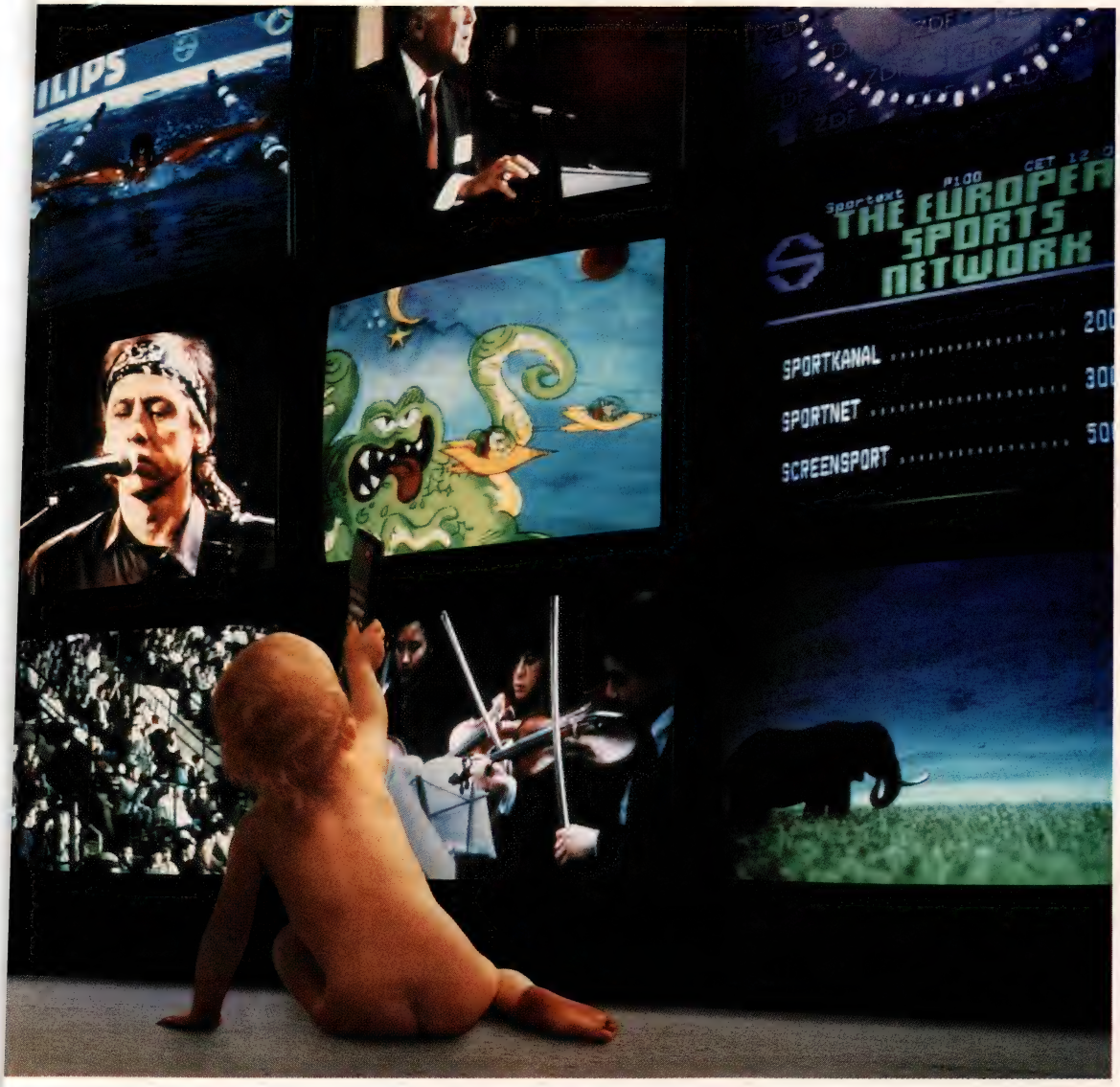
Signetics 80C51—Runs to 33 MHz; has 90-nsec ext-memory-access time. In 40-pin DIP or 44-pin QFP.

SUPPORT

☐ **HARDWARE** The 8051/52 family has many hardware debugging tools. Several ICEs are also available. Piggyback and DIP chip versions are available from Oki, Signetics, and others for debugging and prototyping ROM chips. Siemens has integrated the 8052 with EEPROM on a standard-pinout Macrochip for debugging.

☐ **SOFTWARE** Numerous software tools exist for the 8051/52 family. These tools include assemblers; C, Pascal, and Modula-2 compilers; Forth interpreters; and real-time OS kernels. For slower tasks, engineers can use Basic. (There are public-domain versions of Basic available from Intel and Signetics, as well as at least two first-rate Basic interpreter/compilers, which minimize the need to know assembly-language details.)

WHO IS CREATING THE NEXT GENERATION OF HYBRID ICs FOR CABLE TELEVISION?



able. And for the next generation, Philips is sampling 1 GHz chip capable of providing up to 150 channels.

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It's a role we'll continue to play in the future.

PHILIPS

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CIRCLE NO. 35

Microchip PIC 16Cxx/17Cxx

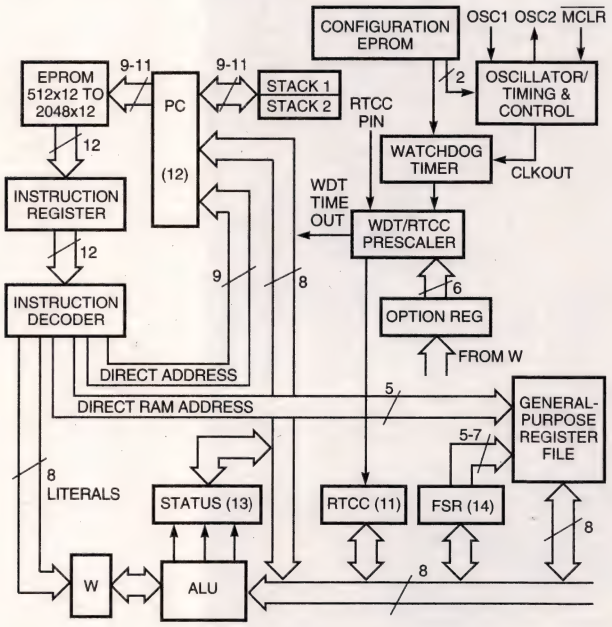
- Harvard architecture; 8-bit data, 12/16-bit (1 word) instr
- RISC-like CPU—2-stage pipeline, 33/55 instr
- Reg-file oriented, no RAM
- 80 to 248 8-bit regs
- 512 bytes to 2 kbytes program EPROM/ROM/OTP memory
- 17Cxx accesses ext memory, 64-kbyte addr space
- Up to 20-MHz (16Cxx), 16-MHz (17Cxx) clock; divide-by-4 internal; static
- 1-cycle instr execution (200/250 nsec, pipelined)
- 400/500-nsec branch
- No MPY, DIV instr
- Software MPY, DIV
- Watchdog timer: 18 msec/2.5 nsec at 20 MHz
- 158-nsec ext-memory access (17C42)
- 20-μsec 8-bit ADC (16C71)
- 750-nsec intr latency (17Cxx)

□ OVERVIEW Microchip Technology's PIC μCs combine a Harvard architecture with RISC-like features to deliver 5-native-MIPS performance in a low-end μC. Originally a mainframe peripheral controller, the PIC has migrated to embedded control. It is the fastest low-end, 8-bit μC around, and Microchip has shipped more than 100 million units. The two mainline PIC families are the 16Cxx and the new 17Cxx, which has a more robust architecture and more peripherals. Both families lack multiply and divide instructions. Most 16Cxxs also lack interrupts, but the 17C42 has 11, including 2 external interrupts. Later PICs have a 32-kHz secondary clock for low power dissipation. The 16C71, introduced in 1992, adds a 4-channel, 20-μsec, 8-bit A/D converter; interrupts; and a new core to the 16Cxx.

□ VENDORS/PRICING Microchip is the sole source.

16C54 (20 MHz, 32 bytes RAM, 512 words EPROM, 18-pin DIP/SOIC/SSOP), $2.11. 16C57 (20 MHz, 80 bytes RAM, 2k words EPROM, 28-pin DIP/SOIC/SSOP), $3. 16C71 (20 MHz, 1k word EPROM, 36 bytes RAM, 18-pin SOIC), $3.25. 16C76 (20 MHz, 80 bytes RAM, 2 kbytes EPROM, 18-pin DIP/SOIC/SSOP), $2.42. 17C42 (16 MHz, 232 bytes RAM, 2k words EPROM, 40-pin QFP/44-pin PLCC), $6.25.

ARCHITECTURE



PIC μCs deliver fast operations with a stripped-down, minimal architecture. The RISC-like CPUs have a 2-stage pipeline, a minimal instruction set, and register-oriented operations. The 16Cxx implements 33 instructions; the 17C42, introduced in 1991, has 55 instructions; the new 16C71 has 35.

The architecture is not new—it has evolved over time from a CPU I/O controller. The latest versions, the 16Cxx and 17Cxx, take advantage of higher chip densities and implement a pipeline with fetch and execute stages. The CPU's Harvard architecture provides separate paths for data and instructions. The data paths are 8 bits wide; the instruction paths are 12 and 16 bits wide for the 16Cxx and 17Cxx, respectively. The 16C71 has a 14-bit instruction word.

The wide instruction word gives the PIC an advantage over many 8-bit μCs. Instructions are held in a single word, so most require a single instruction fetch and execute in a single pipelined cycle. Branches, as in most RISC processors, take an extra cycle.

The PIC 16Cxx has no provisions for external memory. Code must make do with 32 to 80 registers ordered in banks and 512 bytes to 2 kbytes of on-chip program memory. On-chip-memory size, especially RAM, limits the PIC's range of applications. There are instructions to move data held in program memory—typically constants—to registers for processing. The 17C42 has 232 registers and can access external program memory with or without internal EPROM. The external bus is multiplexed—16 bits address, 8 bits data.

Multiple register sets make for fast context switching, but there are limits on subroutine-call depth. PIC CPUs have an automatic stack that holds the current PC for subroutine call/returns. The 16Cxx stack is only 2 deep (except for the 16C71's stack, which is 8 deep); the 17Cxx's is 16 deep.

Working register—Most 2-addr instr, such as arithmetic and logic operations, use the working reg as one of the sources and as destination. Reg functions as an accumulator, eliminating need for two operand accesses to reg RAM.

Interrupts—Early PIC μCs lack intr processing. The 17C42 and 16C71 implement intr. On an interrupt, PC is pushed onto stack and control passed to intr vectors. Need a polling loop on earlier 16Cxxs to test for events.

Table instructions—Enable code to move constants held in program memory to regs for use. Data can be accessed and stored in 17C42's ext memory as well; a holding reg buffers data between memory and regs.

Compare and skip (17Cxx)—Saves code. 16Cxx has decrement-and-skip-on-0 instr.

□ PERIPHERALS/VARIATIONS

Start-up timer—Stabilizes oscillator; 18-msec timeout.

Programmable oscillator—4 options selectable by EPROM fuses: dc to 40 kHz, 4 MHz; 400 kHz to 4 MHz; 4 to 20 MHz.

8-bit timer/counter (16Cxx)—Has 8-bit prescalar. Runs with oscillator÷4 clock as timer or with ext clock as counter (programmable edges). Also watchdog timer.

16-bit timer/counters (17C42)—One 16-bit counter can be divided into two 8-bit ones. Also, two 16-bit capture regs.

PWM (17Cxx)—2 PWM outputs with double-buffered regs to eliminate glitches. 10-bit resolution with programmable operation.

8-bit ADC (16C71)—4-input-channel, successive-approximation converter; 20-μsec conversion. Can be turned off in sleep mode.

Sleep mode—Controller wakes up with reset or watchdog-timer overflow. RAM retained down to 1.5V.

USART (17C42)—Full-duplex asynchronous, or half-duplex, synchronous mode. Has 8-bit baud-generator counter.

I/O-pin drive/sink—I/O pins can drive LEDs directly with 25-mA I/O sink current. I_{LOW}=9.2 mA; I_{HI}=3.4 mA.

Mode	Current (max)	Voltage (V)	Clock (MHz)
Run (17C42)	24 mA	5	16
Run (16C71)	20 mA	5.5	20
Run (16C71)	70 μA	3	32 kHz
Sleep (17C42)	25 μA	5	0
Sleep (16C71)	14 μA	3	0

17C42 in 40/44-pin static DIP;
16C71 in 18-pin static DIP/SOIC.

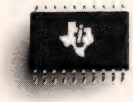
SUPPORT

□ HARDWARE For debugging, you can run the 17C42 in microprocessor mode with 64-kbyte code address space, bypassing on-chip EPROM. Microchip offers an ICE with pods for both PIC families. EPROM burners are available from Microchip and third-party vendors.

□ SOFTWARE Microchip sells a macroassembler/linker/loader. The family has no C compiler yet, but Microchip claims to be working on one. However, the PIC architecture is probably a tight fit for a stack-oriented language like C, given the controllers' limited RAM and stack space.

Which Analog DSP Interface uses 50% less power, fewer components and only one supply?

The new Voice-band Audio Processor from TI.



Our new single-chip Voice-band Audio Processor integrates all the functions of a conventional codec, the amplification for speaker and microphone and more. As a result, you reduce component count and simplify your design.

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TCM320AC37 Highlights

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- Low power: 40 mW (on), 1.2 mW (standby)
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- Pin-selectable 13-bit linear or 8-bit companding
- On-chip interface to speaker and microphone
- Direct interface to most DSPs
- Low cost: < $4.50 (1,000s)

- **Size/Weight** — Eliminating the need for a negative supply and regulator reduces weight and design size. And small-outline surface-mount packaging is available for size-critical applications.
- **Talk time** — Lower power consumption of the 'AC37 allows longer talk time or the use of smaller batteries in your design.

For a free sample and more information
On our TCM320AC37, use the reader service number below.

TEXAS INSTRUMENTS

00-7445B

CIRCLE NO. 37

□ **OVERVIEW** Motorola's 68HC05 leads the 8-bit-μC pack in units shipped. The accumulator-based μC is a minimal design that has few registers and a clean instruction set. Motorola uses the μC as a base for semicustom products for a wide range of industries including consumer electronics, communications, industrial control, automotive, and TV products. There are more than 130 68HC05 variations, many of which started out as semicustom designs. Motorola is now challenging 4-bit-μC vendors with its 68HC05K μC series—a stripped-down 678HC05 crammed into a 16-pin package that costs less than $1 in large volumes.

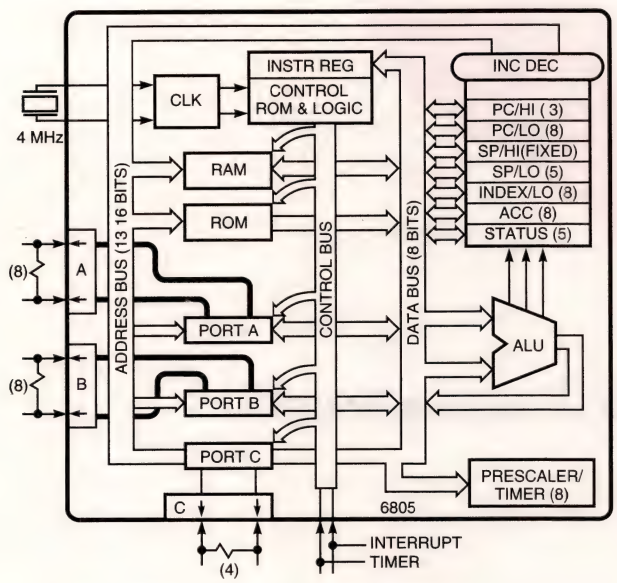
□ **VENDORS/PRICING** Motorola developed the 68HC05; Harris, Hitachi, and SGS Thomson are second sources.

Motorola: 68HC05K0, $1; 68HC05K1, $2.75; 68HC05CC1 (closed-caption controller), $7 (50,000).

Motorola 68HC05

- Accumulator-based CPU
- Accumulator, index, PC, SP, condition-code regs
- 62 instr
- 32 bytes to 1.2 kbytes RAM
- 512 bytes to 16 kbytes ROM/EPROM
- No ext memory
- 64-kbyte addr space
- Watchdog, 16-bit timers; PWM
- 8-bit ADC
- 1 ext intr
- Up to 40 I/O pins
- More than 100 variations, some custom
- DC to 8-MHz clock (divide-by-2 internal)
- 1-μsec ADD, NOP
- 1.5-μsec reg decrement/ increment
- 5.5-μsec MPY
- 8-bit PWM, to 15.6 kHz
- 151.072-kbps transfer rate max for serial communications interface
- 57- to 459-μsec watchdog-timer period
- 10.5-μsec intr latency

ARCHITECTURE



The 68HC05 is a low-end μC with a stripped-down 6800 instruction set. The minimal CPU core has an accumulator, index register, stack pointer (SP), 5-bit condition-code register, and program counter (PC).

The instruction set is regular and easy to write code for. It features straightforward and uncomplicated addressing and 10 addressing modes including 8- and 16-bit indexing from the PC. The PC is up to 16 bits wide to accommodate large address spaces, but RAM is restricted, ranging from 32 bytes to 1 kbyte. Program memory can be as large as 32 kbytes of ROM/EPROM.

The 68HC05's small on-chip RAM limits the on-chip stack to 64 bytes, or 31 calls. Each subroutine call results in the PC being pushed onto the stack. A return pops the PC and resumes execution at the instruction following the original subroutine call.

68HC05 programs generally run from on-chip memory. The 68HC805C4 and the 68HC05A6 can also access and execute from external memory. These chips are primarily used for debugging and prototyping code.

The 68HC05 timer/counter is built around a 16-bit free-running counter, which is coupled with a 16-bit capture register and a 16-bit compare register. The capture register captures timer values on some line events; the timer/counter continually compares the compare register with the running timer. When the registers match, an output-compare flag is set and an output pin driven to a programmed value.

Motorola uses the 68HC05 as a base for a wide range of application-specific μCs. These lines include analog I/O controllers with an on-chip voltage-charge pump and A/D and D/A converters; display-driver controllers with LCD, LED, and TV-screen drives; telephone microcontrollers with DTMF and tone generators; and smart-card controllers with security features.

Stop/wait modes—Wait mode stops CPU processing but leaves the clock, timer, serial-peripheral-interface, and serial-communications-interface systems enabled. Stop mode stops the clock and all internal processing. Both modes maintain RAM and enable intr to wake up the CPU. Most special peripherals are programmable and can be selectively turned off to save power.

Increment/decrement—Can increment or decrement memory or the accumulator or index regs.

Bit operations—Bit-set, bit-test, and branch instr. Bit operations are valid for the first 256 bytes of RAM. Can test and branch on intr bit, but branches are ±127 bytes relative to the PC.

68HC05K1

Mode	Current (max)	Voltage (V)	Clock (MHz)
Run	206 mA	5	4
Wait	0.9 mA	5	4
Stop	1 μA	5	0

In 16-pin DIP, SOIC.

□ **VARIATIONS/PERIPHERALS**

Standard peripherals—8-bit ADC, EPROM/EEPROM program memory, serial communications interface, synchronous serial interface (a 2-wire master-slave system), I²C bus, PWM, timers.

68HC05K series—Low-end μC in 16-pin package. 10 I/O pins, watchdog timer, multifunction timer, 504 bytes EPROM/ROM, 32 bytes RAM. K1 has a 64-bit personality EEPROM.

68HC05CC1—Closed-caption controller. 16,144 bytes ROM; 544 bytes RAM; 31 I/O lines; 8-channel, 6-bit PWM; I²C serial I/O; 1666×9-bit character ROM; on-screen-display module; 40/42-pin DIP.

68HC705C8/C9—μCs for code development and prototyping. C8 has 8 kbytes of EPROM for code; C9 has 2 kbytes of EEPROM.

Special peripherals—DTMF and melody generators; PLL clock multiplier; H-bridge motor drivers; real-time clock; LED display driver; LCD and fluorescent-display drivers; TV on-screen-display unit; serial I/O channels.

SUPPORT

□ **HARDWARE** ICEs for the 68HC05 are available from Motorola and several third-party vendors. Motorola also supplies low-cost hardware development aids and evaluation boards. The 68HC05 Developer's Kit includes an in-circuit simulator that replaces a target μC with a connector that links to a 68HC05 pod that the PC-hosted simulator controls. The PC-hosted simulator drives and inputs the 68HC05K pins, thus letting you run your code in real hardware. The $99 package includes a full development environment.

□ **SOFTWARE** Motorola and third parties supply a wide range of development tools for the 68HC05 including real-time kernels, cross-assemblers, and development environments. There are even C compilers for the limited-RAM chip. Code from one compiler, Bytecraft's (Waterloo, Ontario, Canada) C68HC05, approaches hand-coded assembly code in density.

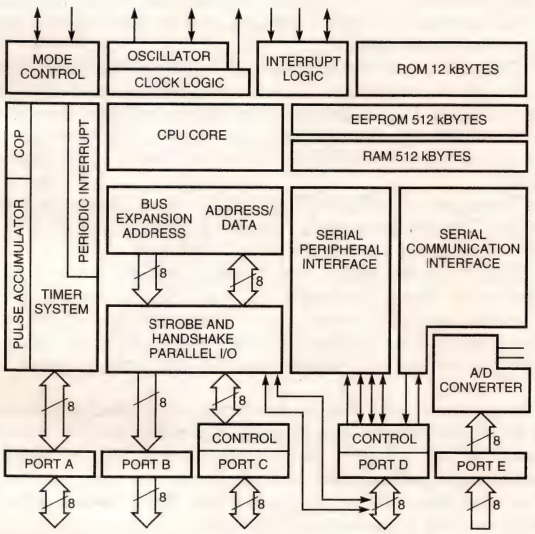
☐ **OVERVIEW** The 68HC11 is the flagship of Motorola's 8-bit μCs. Introduced in 1985, the chip is an upgrade of the 6800/6801 and was initially used in automotive applications. Today, the 68HC11 is popular for embedded applications ranging from industrial control to medical electronics. The accumulator-based μC has up to 24 kbytes of ROM/EPROM, up to 1 kbyte of RAM, and optional on-chip EEPROM. It was one of the first μCs to incorporate sophisticated peripherals such as free-running timers with input-capture and output-compare capabilities. Motorola introduced 3.3V versions in 1992. Family variations include multiplexed or nonmultiplexed external buses, math coprocessors, PWM, ADCs, serial communications, and extended memory (address space can extend to 1 Mbyte).

☐ **VENDORS/PRICING** Motorola developed and sells the 68HC11; Toshiba is a second source. Motorola prices: 3-MHz 68HC11A8, $7.94; 3-MHz 68HC711E9, $9.15; 3-MHz 68HC11D3, $4.20; 4-MHz 68HC11K4, $15.86 (50,000).

Motorola 68HC11

- Accumulator-based CPU
- 2 accumulator, 2 index, SP, PC regs
- 62 instr
- 8 to 32 kbytes ROM/EPROM
- 256 bytes to 1.25 kbytes RAM
- Up to 640 bytes EEPROM
- 64-kbyte addr space, 1 Mbyte expanded
- 16/19-bit ext addr bus, 8-bit ext data bus
- Watchdog timer
- Free-running timer/counter with 4 capture and 4 compare regs, pulse accumulator, four 8-bit PWMs
- 3 ext intr
- Up to 62 I/O pins
- Up to 16-MHz ext clock (4-MHz internal), static
- 500-nsec NOP
- 500-nsec reg-reg ADD; 750-nsec reg-memory ADD
- 750-nsec branch-on-equal
- 5-μsec MPY; 8.25-μsec DIV (coprocessor)
- 1-clock ext-memory cycle
- 40-kHz PWM; 4 channels, 8-bit resolution
- 8-μsec A/D conversion (8/10 bits)
- 14-μsec intr latency

ARCHITECTURE



The 68HC11 is a first-generation, accumulator-based μC. Its popularity rests not on its performance but rather on its range of peripherals and its adaptability. All versions have a basic set of peripherals that includes an 8-bit ADC, 2 serial ports, a free-running timer/counter with capture/compare capabilities, RAM, ROM, and nonvolatile EEPROM.

The 68HC11 has two 8-bit accumulators, two 16-bit index registers, a 16-bit SP, and a 16-bit PC. The CPU can access index registers as high or low bytes and can address the 8-bit A and B accumulators as a single 16-bit accumulator, D. The instruction set is simple and straightforward. It includes many op codes because instruction names reflect the registers used. Addressing modes are limited. There is no base+register addressing, but addresses can be displacement+index.

Addressing is restricted to a 64-kbyte unified address space. Some μCs have a memory-extension unit that expands addressing up to 1 Mbyte. This unit operates a bit like the IBM PC world's expanded memory. Two memory windows in the 64-kbyte address space are mapped into a 1-Mbyte space. The CPU can directly access memory-mapped I/O.

Motorola pioneered using nonvolatile EEPROM in 8-bit μCs. Most family members feature EEPROM, which you can program for embedded IDs, factory test data, calibration data, special application encodings, chip configurations, or operating modes. In effect, the chip is customer configurable without having to go through the program-ROM cycle. Accessing EEPROM is like accessing program memory; the only difference is that reprogramming EEPROM is easy. An on-chip charge pump enables chip-level voltages to program the part.

68HC11s can run using only on-chip memory resources or using I/O ports to access additional external memory. Both multiplexed- and nonmultiplexed-external-bus versions are available. One option available with some units is programmable chip selects, which helps eliminate glue logic by selecting the proper memory bank.

Stack—Push and pop instr put on or take off stack items, automatically adjusting the SP. Wait-for-intr increments the PC, puts all regs on the stack, halts, and waits for an intr. Jumping to a subroutine and returning from a subroutine pushes or pops the PC. Return-from-intr reloads the regs. Software intr also stores the regs in the stack.

Special instructions—Decrement and increment instr for accumulators, index regs, and SP. Operations for speeding code include swapping accumulators, exchanging D accumulator and an index reg, transferring SP+1 to an index reg, comparing memory and 16-bit reg, and setting the SP from an index reg. Bit operations test and set bits using a word mask.

68HC11K4

Mode	Current (max)	Voltage (V)	Clock (MHz)
Run	44 mA	5	16
Wait	22 mA	5	16
Stop	55 μA	5	0

In static 84-pin PLCC, windowed 84-pin PLCC, 80-pin QFP.

☐ VARIATIONS/PERIPHERALS

All versions have ADCs, serial peripheral interface, serial communications interface, complex timer/counter, watchdog timer.

MC68HC11A8—8 kbytes ROM, 256 bytes RAM, 512 bytes EEPROM, pulse accumulator, 38 I/O pins.

MC68HC11E9—12 kbytes ROM, 512 bytes RAM, 512 bytes EEPROM, pulse accumulator, 38 I/O pins.

MC68HC11L6—16 kbytes ROM/EPROM, 512 bytes RAM, 512 bytes EEPROM, pulse accumulator, 38 I/O pins.

MC68HC11N4—24 kbytes ROM/EPROM, 768 bytes RAM, 640 bytes EEPROM, 2 DACs, math coprocessor, 62 I/O pins.

MC68HC711K4—4 chip selects, 24 kbytes ROM/EPROM, 640 bytes EEPROM, 768 bytes RAM, 1-Mbyte ext addressing space, four 8-bit PWMs, 62 I/O pins (8 input only).

Special peripherals—8/10-bit ADC; synchronous serial peripheral interface with 3 wires and master/slave capability; serial-communications-interface USART with parity, noise detection, and 13-bit prescalar. Four-channel, 8-bit PWM to 40 kHz with 1% duty-cycle resolution; two 8-bit counters can form a 16-bit PWM. Math coprocessor can do 16×16-bit MPY, 32/16-bit DIV, 16×16+32-bit MPY-accumulate. Memory-expansion unit can increase addressing to 1 Mbyte.

SUPPORT

☐ **HARDWARE** The 68HC11 is well supplied with hardware tools. You can choose from a range of ICEs, development and evaluation modules, and low-cost single-board computers and logic analyzers. Standard device programmers can program 68HC11 EPROM versions. The μC has a self-programming mode as well, which lets you program the chip on the target board.

☐ **SOFTWARE** The 68HC11 has a large base of development and operating software. Development tools include cross-assemblers, C and Modula-2 compilers, a Forth system, and simulators that run code on host systems. Source and symbolic debuggers are also available. ROM monitors let you debug code from a PC host, and real-time kernels provide multitasking operation.

□ **OVERVIEW** National Semiconductor's COP8 is a first-generation 8-bit μC. The accumulator-based architecture includes a small set of registers and is well suited for low-end control applications. The controller is a static design and can run at voltages as low as 2.5V. Chips come in packages with as few as 20 pins and cost less than $1 in large volumes. COP8 peripherals include 16-bit timers, ADCs, brown-out detectors, PWMs, UARTs, and Microwire/Plus—a serial link to multiple devices or CPUs. The COP8 also serves as a core for application-specific processors.

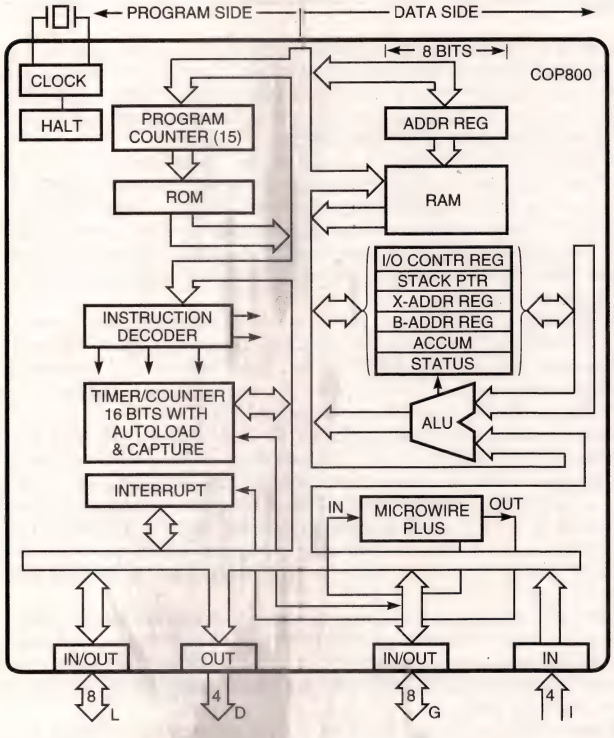
□ **VENDORS/PRICING** National Semiconductor developed the COP8 and is the sole source.

COP820CJ (1 kbyte ROM, 64 bytes RAM, 16-bit timer, watchdog timer, brown-out detector, analog comparator, LED driver), $1.33; COP820C (1 kbyte ROM, 64 bytes RAM, 16 I/Os, 20-pin DIP), $1.15; COP880C (4 kbytes ROM, 128 bytes RAM, 36 I/Os, 44 pins), $1.45; COP888EG (8 kbytes ROM, 256 bytes RAM, 2 analog comparators, Microwire/Plus serial interface, UART, 39 I/Os, 44 pins), $3.05.

National Semiconductor COP8

- Accumulator-based CPU
- 6 to 8 8-bit regs: A, B, X, SP, PSW
- 44 to 55 instr
- 64 to 256 bytes RAM
- 1 to 8 kbytes ROM
- 32-kbyte addr space
- Microwire/Plus serial interface
- 16-bit timer with autoload, capture
- Watchdog timer
- Brown-out detector
- 1 ext intr
- Up to 39 I/O pins
- 10-MHz ext clock (1-MHz internal)
- 1-μsec ADD, NOP
- 3-μsec JUMP, PUSH, POP
- No MPY/DIV
- Accesses ext memory serially in ROMless mode
- 500-kHz Microwire/Plus serial burst rate
- High-current I/O directly drives LEDs
- 2.3 to 6V parts
- 7-μsec intr latency

ARCHITECTURE



A first-generation μC, the COP8 combines a minimal architecture with low-cost peripherals and as few as 20 pins. The controller, which has no multiply or divide instructions or complex addressing, is used primarily in low-end commercial and industrial control.

The COP8 is an accumulator-based architecture, and all data operations must go through an accumulator. There are 6 to 8 control and data registers, including the accumulator. All registers are memory mapped except the accumulator. The COP8 registers include the 8-bit accumulator, two 8-bit address registers, and a 15-bit PC, which the CPU can access as upper and lower 8-bit registers.

The μC executes an ADD, SHIFT, or LOAD in one internal clock cycle (1-μsec period). The instruction set is relatively simple—more than 70% of the operations execute in 1 clock and take up only 1 byte.

The COP8 is a static design, and its clocks can be slowed to minimize power dissipation. Two power modes—halt and idle—further cut power losses. Idle restricts peripheral operations; halt stops the clock. COP8s can run with external memory for debugging and prototyping code. An 8-bit port serially reads from and writes to external memory and provides emulation control.

COP8s can handle critical tasks: A watchdog timer catches runaway software; a brown-out detector detects power-loss conditions that can threaten safe operation; and all software-generated errors, such as illegal ROM addresses or stack overflows, automatically cause a software interrupt or trigger a processor reset. These safeguards ensure that software or hardware errors will not cause indeterminate conditions.

Stack—Intr and subroutine calls push PC onto stack and upgrade SP. Stack resides in RAM, limiting call and intr depth. Return from intr or subroutine returns control to next instr.

Addressing modes—Reg indirect (reg specified in operation), direct (8-bit addr field), immediate (8-bit value in instr), relative (local jump –31 to +32 locations).

Special instructions—Test-and-skip instr eliminates code. Can test for a condition, and if not true, skip condition processing in next instr. Increment and decrement instr for accumulator. Also bit-set and -reset and bit-test-and-skip instr.

□ PERIPHERALS

Analog comparators—Can be used to build rough ADC.

Brown-out detector—Detects voltage drop below brown-out voltage and causes a reset, restarting the CPU.

Microwire/Plus serial port—Serial synchronous, bidirectional interface links μC to other processors or peripheral chips via serial protocol. Ext or internal serial-shift clock. Configured via bits and fields in control reg.

Timer/counter—Can have up to 3. Timer/counter 1 can be autoload counter (counts to 0, reload), external counter (triggered by ext signal), or capture counter (captures counter value into reg on an ext signal).

EEPROM—64 bytes EEPROM in RAM space for nonvolatile storage.

Multi-input wakeup—Transition on an L-port pin wakes μC from halt mode. Triggering bits and their transitions are programmable.

Mode	Curent (max)	Voltage (V)	Clock (MHz)
Run	8 mA	5	10
Halt	10 μA	5	0

In 20/28-pin DIP, 16-pin SOIC.

SUPPORT

□ **HARDWARE** Piggyback emulation chips (EPROM piggybacked on DIP) are available for some versions, as are hybrids with built-in EPROM for debugging. ICEs and low-cost evaluation boards are available from National Semiconductor and at least one third-party vendor.

□ **SOFTWARE** National Semiconductor supplies assemblers and linkers for the COP8 as well as a simulator for host debugging. ByteCraft (Waterloo, Ontario, Canada) has built a C compiler for the controllers, which it and National Semiconductor sell. National Semiconductor has integrated neural nets and fuzzy-logic technology into a COP8 development tool due out in 1993.

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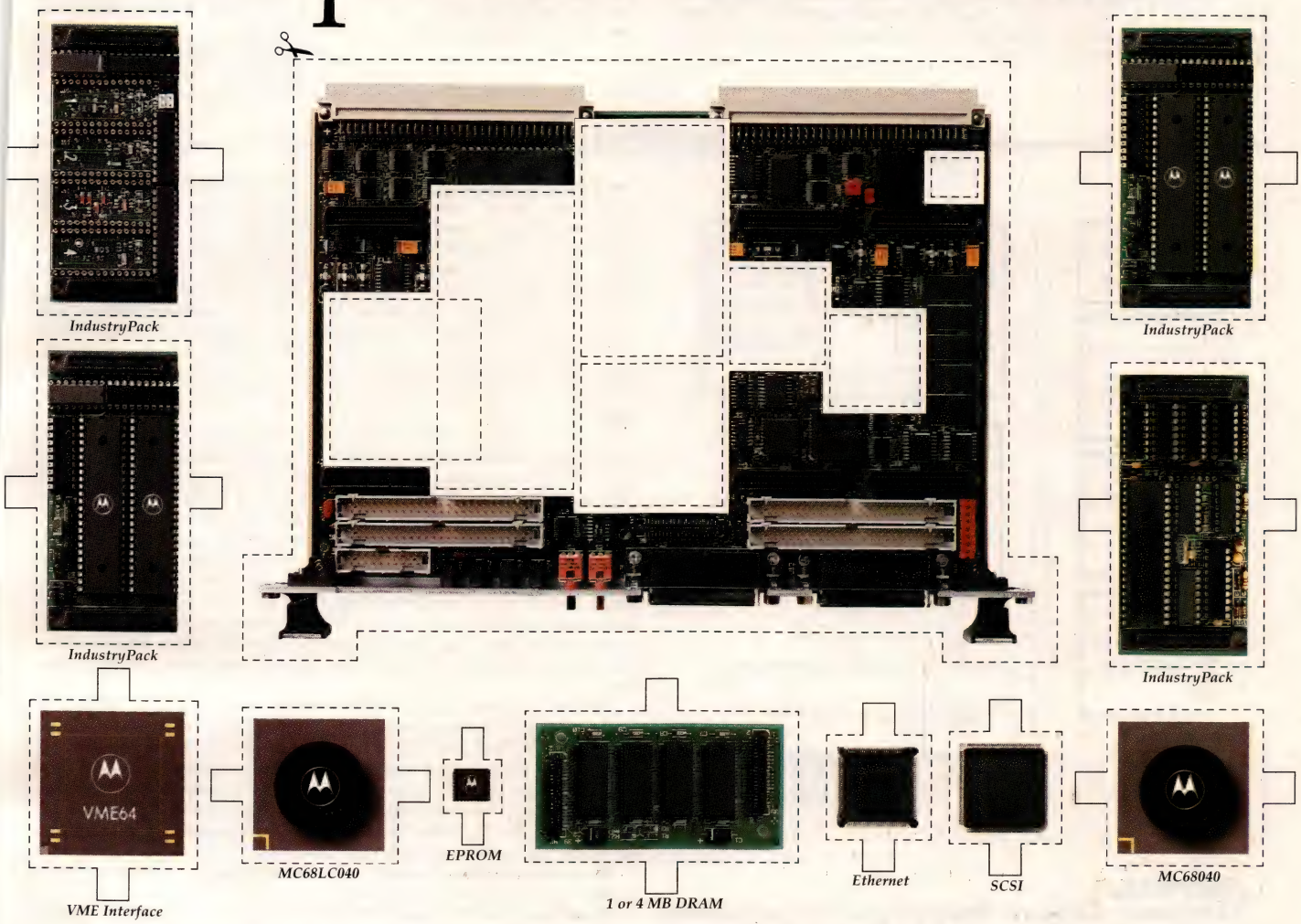

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□ **OVERVIEW** The NEC 78K series comprises three μC lines: The K2 is a midrange 8-bit, 12-MHz chip with a full set of peripherals. The newer K3 is a 16-bit μC running at 12 to 32 MHz and has more complex timers, fast A/D and D/A converters, and a MPY/accumulate instruction. The K0 line, introduced in 1992, is built on a K2 base and brings 4-bit peripherals to 8-bit processors. The K0/K2 and the K3 are not code compatible, but code can easily be moved between them. The K0 operates down to 2.7V for low-power applications. The K2 and K3 have a macro service, which offloads the CPU by handling peripheral events including DMA data transfers. Packages range from 64-pin DIPs to 100-pin QFPs. 78K-series μCs target mass-storage, automotive, motor-control, and portable applications.

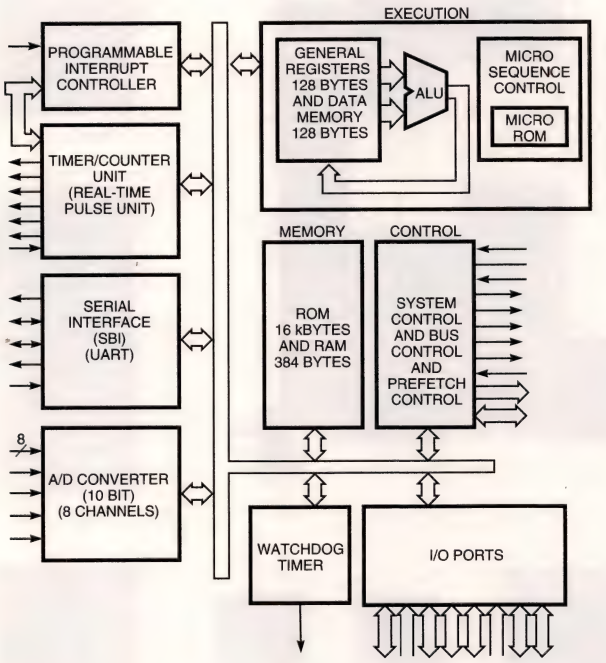
□ **VENDORS/PRICING** NEC is the developer and sole supplier.

78356 (32 kbytes ROM, 2 kbytes RAM, 5 timer/counters, 10-bit ADC, 2 DACs, UART, 54 I/Os), $14 (sampling); 78011 (8 kbytes ROM, 256 bytes RAM), $5.50; 78214 (16 kbytes ROM, 512 bytes RAM, 8-bit ADC, UART, 4 timer/counters, 54 I/Os), $7.20.

NEC 78K

- K2/K0, 8-bit μCs; K3, 16-bit μC with same basic architecture
- Reg-block oriented: 4 banks of 8 8-bit regs (K2, K0); 8 banks of 8 16-bit regs (K3)
- Up to 48 kbytes EPROM/ROM; 256 bytes to 2 kbytes RAM
- 64-kbyte addr space (K3); 64-kbyte code, 1-Mbyte data space (K2)
- Macro peripheral service
- 4-bit peripherals (K0)
- MPY/ACCUM instr (K3)
- 12- to 32-MHz clock (divide-by-2 internal), K2/K3
- Up to 10-MHz programmable clock, 32-kHz subclock (K0)
- 188-nsec ADD; 875-nsec MPY (32-MHz K3)
- 2.69-μsec DIV; 1.31-μsec MPY-ACCUM (32-MHz K3)
- 333-nsec ADD, 3.6-μsec MPY (12-MHz K2)
- 2-μsec conversions for 10-bit A/D, 8-bit D/A converters (78356)
- 500/180-nsec ext R/W (K2/K3)

ARCHITECTURE



The NEC 78K series includes 8- and 16-bit implementations of a common architecture. The μCs operate on banks of registers. The 8-bit K2 and K0 (a derivative of the K2) center around 4 banks of eight 8-bit registers; the K3, a 16-bit μC, has a base of 8 banks of eight 16-bit registers. A field in the PSW (program status word) denotes the current register bank. Context switching is easy—only the PSW current register-bank field needs to change.

In both architectures, the register banks are in on-chip RAM along with directly accessible RAM. The CPU addresses the registers symbolically as the current register bank or as memory. Both the K2 and K3 implementations separate RAM into fast RAM inside the execution unit with the ALU and separate data RAM. The fast RAM includes 128 bytes of register and 128 bytes of data RAM.

The K2 accesses a 64-kbyte program address space and up to 1 Mbyte of data space. Its multiplexed external bus has 16-bit addresses and 8-bit data buses. A 4-bit expansion (A16 to A19) opens up addressing to 20 bits, or 1 Mbyte. The K3, in contrast, limits addressing to a single 64-kbyte address space and has an 8- or 16-bit multiplexed external memory bus.

The K0 is built on the K2 base and drives portable and low-power applications. It runs a subset of the K2 code but is a slower part. It has a dynamically adjustable internal clock. While running, the clock speed can be divided by 2, 4, 8, or 16. Additionally, like many 4-bit μCs, the K0 can switch to a secondary 32-kHz clock and wait in low-power mode for a interrupt event to resume execution. The 78K0 parts do not have the macro peripheral service, which offloads the CPU by processing peripheral events and data transfers.

The 8-bit K2 handles 16-bit operations by pairing adjacent registers in banks. Its 16-bit arithmetic operations include MOVW, ADDW, SUBW, INCW, DECW, and SHR/LW (shift). These operations and register pairing make it easy to do 16-bit addressing in an 8-bit machine with an 8-bit ALU. Conversely, the 16-bit K3 supports 8-bit operations and addresses registers as 8-bit entities. These characteristics make it easy to move 8-bit K2 code to the 16-bit K3. The K3, unlike the K0 and K2, offers user and supervisor modes for separating system and application operations.

Bit manipulation—Set, clear, complement, or test a bit in memory, special-function reg, PSW, or A or X regs.

Stack—In RAM. PUSH or POP the PSW, reg (reg pair for K2, K0), special-function regs.

Interrupts—Handled 3 ways: as vectored calls to service routines; by the macro peripheral service, thus bypassing the CPU; or as a context switch (K3 automatically switches to a new reg bank; K2 needs a bank-select instr and then saves PC and PSW and branches to the ISR referenced in new bank).

Special instructions—Increment and decrement for regs and memory; exchange instr for both regs and memory; decrement reg or memory location and jump if not zero. Hardware implements 32-word branch-destination addr table that adds a level of indirection to branches and subroutine calls.

□ PERIPHERALS

K2/K3 macro peripheral service—Programmable service handles I/O events directly instead of using intr to schedule CPU. Triggering events include timer match, input-pin signal edges, ADC completion, termination of serial-interface peripherals. Service moves byte, word, blocks of data.

K3 10-bit A/D, D/A converters—Programmable A/D converter with 8 input channels, 2-μsec conversion. Converter can be triggered by ext signals (including pulse that triggers each input-channel A/D conversion), software, or timer events. Two D/A converters have 2.0-μsec settling time.

K3 MAC instruction—78356 has a MAC (multiply-and-accumulate) instr that multiplies 2 numbers and puts result into a running accumulator. Not a separate MAC unit, but an implementation that's faster than assembling instr. Loop mode for iterative calculations.

8-bit real-time port—Data stored in buffer reg is output to a port on a specific timer or interrupt event. Configured as one 8-bit channel or two 4-bit channels.

K0 dynamic clock—Like 4-bit μC, the K0 can dynamically drop execution down to a low-power, 32-kHz subsystem clock while waiting for an event. Can dynamically reprogram main clock, dividing it by 2, 4, 8, or 16.

78014

Mode	Current (max)	Voltage (V)	Clock (MHz)
Run	22.5 mA	5	8.38
Halt	4.2 μA	5	8.38
Stop	20 μA	5	0

In 64-pin DIP, QFP.

SUPPORT

□ **HARDWARE** NEC has an ICE for 78K series chips. Evaluation boards are available for most versions.

□ **SOFTWARE** Development tools include a macroassembler/linker and a C compiler. The macroassembler has high-level-language constructs that simplify assembly-language programming.

☐ OVERVIEW

Introduced in 1975, the 8-bit 6502 still lives and prospers. A derivative of Motorola's 6800, the 6502 was one of the first successful μPs and served as the base for a number of popular early personal computers, such as the Commodore PET and Apple II. The 6502 and its descendants now serve as embedded controllers for a wide range of applications. Mitsubishi's 6502-based 37400 μC is a popular 8-bit chip in Japan. Rockwell sells 6502 μPs as well as 6500/x μCs built around the CPU. Rockwell's 6502-based CMOS controllers are a major presence in modems and fax machines. Western Design Center also sells a CMOS 6502 μP and μCs, as well as 16-bit extended μPs.

☐ VENDORS/PRICING

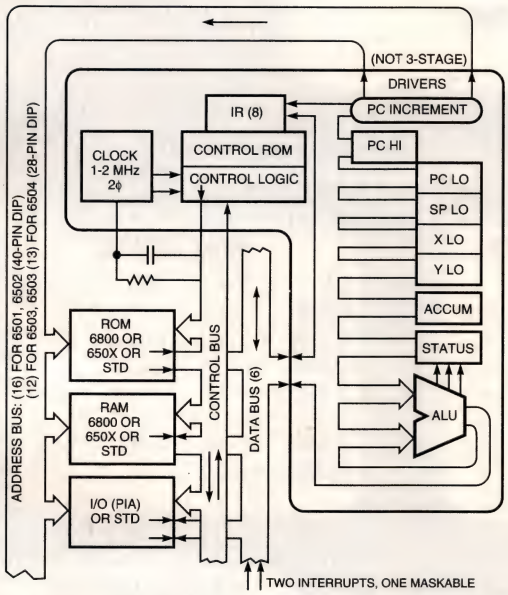
Several vendors make 6502/6500 parts.

Mitsubishi: M37451MC-XXXFP (6502 μC, 24 kbytes ROM), $9; M37471M2 (6502 μC, 4 kbytes ROM), $5. Rockwell: R65C02, $2.25; R6500/1 (2 kbytes ROM), $4.16; R6500/12 (3 kbytes ROM), $7.49; R65C19 (16 kbytes ROM), $6.25. Western Design Center (1000): W65C02S (enhanced 6502, 10 MHz), $9.26; W65C134 (6502 μC, 4 kbytes ROM), $13.12; W65C816S (10 MHz, 16-bit 6502 μC), $11.12.

Rockwell/WDC 6502/6500

- Minimal-architecture μP/μC
- 1 accumulator reg
- 2 index regs
- 16-bit PC; 8-bit SP, PSW regs
- 56 instr
- Up to 16 kbytes ROM
- Up to 512 bytes RAM
- 8-bit timer(s)
- 8-bit ADC, DAC (some chips)
- Extended 16-bit versions
- Up to 56 I/O pins, 6 ext intr
- Rockwell R65C19 μC
- Up to 10-MHz ext, internal clock (although most use divide-by-2 internal clock)
- Some static designs
- 2-cycle NOP
- 2-clock ADD
- 3-clock mem-reg ADD
- 6-cycle MPY
- No DIV (no MPY for most 6502s)
- 8-clock mem-mem move
- 1-clock mem R/W
- 8-clock intr latency

ARCHITECTURE



Created by some of the designers that built the Motorola 6800, the 6502 is a reworked 6800 and was an advanced 8-bit microprocessor for its day. It's a relatively powerful μP crammed onto a very small die and delivers a price/performance ratio that made the chip popular in the early days of personal computers. Today, 6502s are used heavily as embedded controllers for telecommunications, TV, computer peripherals, consumer products, and industrial control.

A first-generation, accumulator-based CPU, the 6502 is a minimal design. It has a single 8-bit accumulator and two 8-bit index registers. The stack pointer is 8 bits wide, but the PC is 16 bits. For speed, the implementation is semi-pipelined: The CPU fetches the next instruction while decoding and executing the current instruction. The 6502's relatively fast memory interface lets code use page-0 RAM as a large register set to hold dynamic variables.

The 6502 has a 64-kbyte, unified address space. This space is divided into 256-byte pages for X, Y indexing. The 0 page is the first page in memory and can be addressed easily via special address modes and instructions. The chip has a fast nonmultiplexed external bus—16 bits for addresses, 8 bits for data.

Western Design Center's 16-bit extension of the 6502, the WC65C816S, is compatible with the 65C02. One extended version, the WC65C802, is even pin compatible with the 65C02. The extended versions have 16-bit accumulator, index, and SP registers. The 16-bit CPU also added 78 op codes, 9 addressing modes, and a second 8-bit accumulator. A 6502-emulation mode lets the 16-bit chip directly execute 6502 object code.

The WC65816 family addresses up to 16 Mbytes of memory; the 6502 has a 64-kbyte limit. The 16-bit CPU generates a 24-bit address by concatenating the 16-bit program or calculated address with an 8-bit bank register. There is a bank register for program and one for data. Mitsubishi has also extended the 6502 architecture to 16 bits. Its 37700 family (see entry) also has a modified architecture.

Stack—The 8-bit SP limits stack to 256 entries, held in fixed location. Hardware automatically pushes/pops PC onto the stack for intr and subroutine CALL/RETs. Application code can use stack for temporary data. Only accumulator and PSW can be pushed/pulled to stack (65C02 added push/pull for index regs). WDC's 16-bit extension has 16-bit SP.

Addressing modes—Implied; accumulator; immediate; absolute; PC relative; stack; 0 page; absolute indexed with X, Y; 0-page indexed with X, Y; absolute indirect; 0-page indirect indexed with Y (post-indexed) or X (pre-indexed). 65C02 has 0-page indirect and absolute-indexed indirect.

Special instructions—Increment, decrement; test memory bits against accumulator; compare regs to memory; push/pull accumulator onto/off stack; push/pull PSW onto/off stack.

New 16-bit instructions—Coprocessor enable; push/pull effective-addr, index regs, bank regs to/from stack; load one index reg from another; block moves; long jumps and returns; stop CPU; wait for interrupt.

☐ VARIATIONS

R65C02 (Rockwell)—4 MHz, 40-pin DIP, 44-pin PLCC.

R6500/1 (Rockwell)—4 MHz, 2 kbytes ROM, 64 bytes RAM, 16-bit counter, 5 ext intr, 32 I/Os, 40-pin DIP, 44-pin PLCC.

R6500/12 (Rockwell)—4 MHz, 3 kbytes ROM, 192 bytes RAM, USART, 2 16-bit counters, 6 ext intr, 56 I/Os, 68-pin PLCC.

R65C19 (Rockwell)—10 MHz, 16 kbytes ROM, 512 kbytes RAM, 4 16/17-bit counters, 8 ext intr, 44 I/Os, 80-pin QFP, 64-pin PLCC.

W65C02S (WDC)—Enhanced 6502; 66 instr, 40-pin DIP, 44-pin PLCC.

W65C134 (WDC)—6502-based μC, static design. 4 kbytes ROM, 192 bytes RAM, 4 16-bit timers, 8-bit data/16-bit addr ext bus, 8 chip select signals, UART, serial-interface channel, 2 programmable clock inputs, 1.2 to 5.5V, 56 I/Os, 68-pin PLCC.

W65C816S (WDC)—16-bit version of 6502. Up to 10 MHz, 16-bit regs, 16-bit SP, 24-bit addr space, 91 instr, 24 addr modes, 40-pin DIP, 44-pin PLCC.

M37451M5-XXX (Mitsubishi)—Expanded 6502 μC. 4 MHz, 16 kbytes ROM, 384 bytes RAM, 3 timers, PWM, serial I/O, 8-bit ADC, 8-bit DAC, UART, 64-pin DIP, 80-pin QFP.

M37471M2 (Mitsubishi)—4 MHz; 4 kbytes ROM; 128 bytes RAM; timer; 8-channel, 8-bit ADC; serial I/O; 36 I/Os; 42-pin DIP.

M38063M8-XXXFP (Mitsubishi)—5 MHz, 32 kbytes ROM, 1 kbyte RAM, 4 timers, ADC, DAC, UART, 72 I/Os, 80-pin QFP.

Chip	Current (max at 5V)	Package	Clock (MHz)
M37451MX	8 mA	64-pin QFP	12.5
R6500/1	240 mA	44-pin PLCC	8
R65C19	60 mA	64-pin PLCC	10
W65C134	24 mA	68-pin PLCC	8

SUPPORT

☐ HARDWARE

ICEs and logic analyzers are available for 6502/6500 chips. Most μC vendors supply piggyback DIPs—DIP chips with a piggyback for EPROM to hold program memory. Evaluation boards are available from chip vendors and third-party suppliers.

☐ SOFTWARE

The 6502/6500 family has a large third-party base of operating and development software. Languages include assembler, Forth, Basic, C, and Pascal. Apple IIs (65C02) and IIgs (65C816) can serve as native development platforms.

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NEW EL2120	100 MHz	2.80
EL4393 triple	82 MHz	6.95
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P/N	GBW	$ @ 100 pc.
NEW EL2044	120 MHz	1.80
NEW EL2244 dual	120 MHz	2.95
EL2444 quad	120 MHz	4.95
NEW EL2045	100 MHz	1.80
NEW EL2245 dual	100 MHz	2.95
NEW EL2073	200 MHz	4.95
EL2074	400 MHz	5.25

VIDEO BUFFERS

P/N	BW	I/O	$ @ 100 pc.
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*V/µs **BW

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*V/µs

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CIRCLE NO. 41

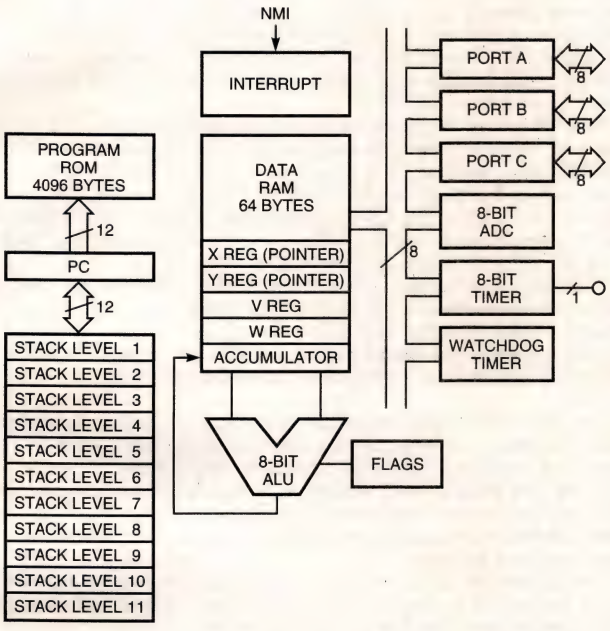
☐ **OVERVIEW** Introduced in 1989, SGS-Thomson's ST6 is a stripped-down, first-generation, accumulator-based μC. The chip targets low-end control and display tasks in automotive, large-appliance, radio/TV, telecommunications/security, and industrial applications. Most ST6s fit into a 20- or 28-pin package, which is ideal for tight-space applications. The basic ST6 die area is 2000 mm², and the chip has a serial implementation to minimize silicon. The architecture is limited to a 4-kbyte program space, which a banking scheme can extend. Chip peripherals include ADCs, timers, and a serial peripheral interface. There are ROM and OTP ST6 versions. SGS-Thomson has expanded the line with higher-pinout μCs for large-display applications. The ST62E40 combines 45 segment outputs and 4 backplane outputs (for 180 LCD segments) with 192 bytes of RAM, 7948 bytes of EPROM, and 128 bytes of EEPROM.

☐ **VENDORS/PRICING** SGS-Thomson developed the ST6 and is the sole source. ST6211, $1.50; ST6210, $1.80; ST6293, $2.70; ST6240, $5.50.

SGS-Thomson ST6

- 5-reg, 8-bit ALU; 12-bit PC
- 6-level automatic stack
- 28 instr
- Up to 512 bytes RAM
- Up to 20 kbytes ROM/EPROM
- 4-kbyte addr space
- 15-bit timer, 8-bit watchdog timer
- 8-channel, 8-bit ADC
- 3 to 6V operation; brown-out detection
- Up to 23 ext intr
- Up to 20 I/O lines; 4 sink 10 mA for LEDs
- 8-MHz ext clock (1 MHz for 3V version), static
- 1.625-μsec instr cycle (13 clocks)
- 6.25-μsec ADD, LOAD
- 3.25-μsec NOP
- 6.25-μsec increment/decrement
- No MPY, DIV
- 70-μsec A/D conversion
- 9.75-μsec intr latency

ARCHITECTURE



A low-end 8-bit μC, the ST6 has 6 registers: 2 index registers (X, Y); 2 general registers (V, W); an accumulator; and a program counter. The PC is 12 bits; all other registers are 8 bits. All basic arithmetic operations involve the accumulator as one parameter and end by placing a result into the accumulator. However, the ST6 is not a classic accumulator-based CPU. Loads are a little more flexible—the accumulator can be either the source or destination. Also, both memory and registers can be incremented or decremented directly without passing though the accumulator.

Registers appear as memory locations in the chip's address space. Instructions can address registers directly as a memory location. Peripherals are memory-mapped; they are also accessible as memory addresses. To configure a peripheral or send or receive data to or from a peripheral, a program simply writes to or reads the peripheral's memory registers.

The ST6 doesn't have a classic stack for holding PC values during subroutine calls or interrupts. Instead, chip architects put in an automatic fixed stack. On subroutine calls or interrupts, the hardware automatically pushes the current PC onto the stack. On return, the hardware pops the PC value off the stack and loads the PC with it. The automatic stack is only 6 levels deep, so you must carefully control subroutine-call depths. If the stack is full and a call or interrupt occurs, the current PC value will be pushed onto the stack and all stack entries will move down one. The last entry (first in) will be lost.

The PC addresses up to 4 kbytes of program memory. A banking scheme that uses a dedicated memory-mapped banking register can expand the program memory. The lower 2 kbytes of ROM can be banked, which would provide access to higher 2-kbyte pages in program memory ranging up to 20 kbytes. Program memory can also hold constants or tables, which the CPU accesses via a 64-byte memory-mapped window in RAM that maps into ROM.

The instruction set is small and relatively straightforward. Relative jumps are restrained to –15 to +16 locations, and there are no complex instructions.

Addressing modes—Inherent (in op code); direct (instr byte); short direct (data in X, Y, V, W regs); indirect (use X, Y as addr); immediate (in last instr byte); PC relative (PC+displacement); extended (12-bit op code+next); bit direct (bit addr); bit test (with –126 to +129 displacement range).

Bit manipulation—Set or reset bits in regs or memory. Test bit with jump relative instr.

Special instructions—Increment/decrement regs or memory; compare A reg to reg/memory byte or constant; clear or complement reg/memory; test and jump operations with –15 to +16 displacement.

ST6210

Mode	Current (max)	Voltage (V)	Clock (MHz)
Normal	3.5 mA	5.0	8
Wait	1.5 mA	5.0	8
Stop	10 μA	5.0	0
Normal	300 mA	3.0	1

In 20/28-pin static SOIC.

VARIATIONS

ST6210—2 kbytes ROM, 64 bytes RAM, 8-bit timer (7-bit prescalar), watchdog timer, 8-bit ADC, 12 I/O pins, 20-pin DIP/SOP.

ST6211—Core ST6 system with 2 kbytes ROM, 64 bytes RAM, 8-bit timer, watchdog timer, 12 I/O pins, 20-pin DIP/SOP.

ST6220—4 kbytes ROM, 64 bytes RAM, 8-bit timer (7-bit prescalar), watchdog, 8-bit ADC, 12 I/O pins, 20-pin DIP/SOP.

ST6293—(4 kbytes ROM, 128 bytes RAM, 128 bytes EEPROM, 8-bit timer (reload, capture, compare regs), 8-bit ADC, serial peripheral interface, 80-pin QFP.

ST6240—8 kbytes ROM, 216 bytes RAM, 128 bytes EEPROM, two 8-bit timers, 8-bit ADC, 180-segment-LCD driver, serial peripheral interface, 32-kHz LCD oscillator, real-time clock, 80-pin QFP.

SUPPORT

☐ **HARDWARE** SGS-Thompson sells an ICE for the ST6 family as well as a gang programmer and an EPROM programming board. An IBM PC parallel port drives the board. The ST6 starter kit includes a software-development package, stand-alone chip programmer for DIPs, samples of EPROM-based ST6 μCs, and power supply.

☐ **SOFTWARE** A single-pass macroassembler and linker is available for the ST6. The tools use the ROM data window for holding constants in program ROM. SGS-Thomson also has a simulator that runs ST6 code on a PC host. The windowed simulator handles symbolic debugging with as many as 128 breakpoints and 128 software traps.

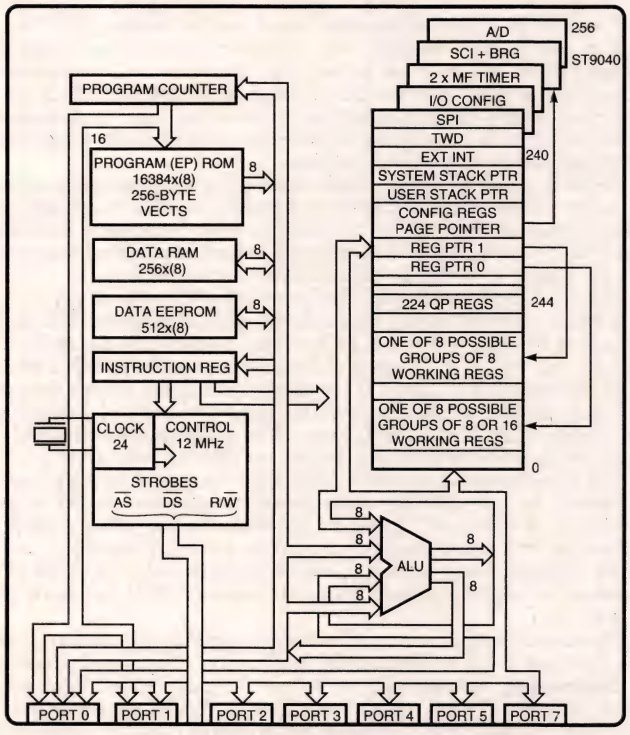
□ **OVERVIEW** SGS-Thomson's ST9 is an 8-bit processor with some 16-bit characteristics. It has an 8-bit ALU but uses a 16-bit instruction word and does both 8- and 16-bit arithmetic, which eases addressing. The ST9 suits high-end 8-bit applications in automotive, white-goods, telecommunications, industrial, and radio/TV control. Driven by a 24-MHz clock, the μC delivers 500-nsec operations and 1.8- and 2.3-μsec multiplies and divides. The ST9's architecture resembles that of the Z8, for which SGS Thomson is a second source. The ST9's 3 address spaces are program, data, and an on-chip register file. Operations are mainly on groups of registers. The processor has ROM, EPROM, EEPROM, and OTP memory. The CPU can dynamically modify on-chip EEPROM for nonvolatile critical storage. The chip itself is shrinking: Originally implemented in 1.5-μm technology in 1987, the ST9 now uses 1.2-μm technology and is moving to 0.8 μm.

□ **VENDORS/PRICING** SGS-Thomson developed and sells the ST9; Siemens is a second source. SGS-Thomson: ST9026, $6.90; ST9030, $7.40; ST90R50, $7.

SGS-Thomson ST9

- Reg-based CPU; 256-byte reg file in RAM, 15 working groups
- 8-bit ALU, 16-bit instr; CPU does 8-, 16-bit operations
- 87 instr
- Up to 1.2 kbytes RAM
- Up to 32 kbytes ROM/EPROM/EEPROM
- 2 64-kbyte addr spaces
- 16-bit addr, 8-bit data ext bus; multiplexed or nonmultiplexed
- Up to 8 ext intr
- Up to 72 I/O pins
- 24-MHz ext clock (12-MHz internal)
- 500-nsec ADD, NOP; 1.67-μsec mem-reg ADD
- 500- to 833-nsec LOAD
- 1.8-μsec MPY, 2.3-μsec DIV
- 250-nsec ext bus cycle, programmable wait states
- 11-μsec 8-bit A/D conversion
- 666-nsec/byte DMA transfer
- 110- to 375-kbaud, full-duplex serial interface
- 2.16-μsec intr latency

ARCHITECTURE



SGS Thomson's ST9 is part of the wave of 8/16-bit μCs taking on high-end 8-bit applications. These controllers feature 8-bit processing but use 16-bit-wide instructions to speed processing. Many 8-bit CPUs slow down to fetch multiple-word instructions. Opcode+displacement is a classic 2-byte instruction and takes 2 memory fetches; a 16-bit instruction takes only 1 fetch. The ST9 has two internal buses: an 8-bit register bus and a 16-bit memory bus, which also moves instructions.

The ST9 is a register-based processor that operates on a selected group or set of 16 registers, but it is not a classic register-based machine. Instead, the ST9 resembles the Zilog Z8 architecture by having 3 address spaces—program, memory, and register file. The ST9's CPU manages the 256-byte register file as 14 sets of 16 8-bit general-purpose registers rather than as one set of general-purpose registers. (The 16th set is the system page, and the 13th set cannot be addressed as a working set.)

Switching from one set or group of registers to another makes for fast context switching because no registers must be saved or restored. Instead, the register pointer changes to reference a new register set. There are actually 2 register pointers in the register file. Each pointer can reference one working bank of 8 registers, or a single pointer can address a working set of 16 registers.

The 244 addressable general-purpose registers can be accumulators, index registers, or address pointers. Adjacent register pairs make up 16-bit registers for addressing or 16-bit processing. Although the ST9 has an 8-bit ALU, the chip handles 16-bit operations, including arithmetic, loads/stores, and memory/register and memory/memory exchanges. Many op codes specify byte or word operations—the hardware automatically handles 16-bit operations and accesses.

On-chip peripherals can transfer data to or from memory or registers via DMA channels, thus offloading the CPU. A DMA channel can move up to 222 bytes to the register file or 64 kbytes to data memory.

Stack—System stack with SP for interrupts or subroutine calls. User stack is under user control with user SP. Stacks in on-chip RAM or off-chip memory. Word- or byte-oriented PUSH and POP operations.

Addressing modes—Reg direct, indirect, indexed; memory direct, indirect, indirect with postincrement/predecrement, indexed with immediate short/long/reg offset; memory indirect postincrement to indirect reg postincrement; memory map to memory map (both postincrement); bit address.

Special instructions—Increment/decrement regs or memory; compare bytes/words; clear/complement reg/memory; test/test-complement under mask (AND destination with mask, test for 0); bit set/reset/complement/test-and-set.

ST9030

Mode	Current (max)	Voltage (V)	Clock (MHz)
Normal	70 mA	5	24
Halt	18 mA	5	24
Stop	100 μA	5	0

In 68-pin PLCC.

□ VARIATIONS

ST9026—16 kbytes ROM/EPROM, 256 bytes RAM, multifunction timer with DMA, watchdog timer, serial communications interface with DMA, serial peripheral interface, 5 I/O ports, 48-pin DIP.

ST9030—8 kbytes ROM/EPROM/OTP memory; 2 multifunction timers; watchdog timer; 8-bit, 8-channel ADC; serial peripheral interface; multichannel DMA; 7 I/O ports; 68-pin PLCC.

ST9040—16 kbytes ROM/EPROM, 256 bytes RAM, 512 bytes EEPROM, 2 timers, watchdog timer, SCSI, serial peripheral interface, 8-bit ADC, multichannel DMA, 7 I/O ports, 68-pin PLCC.

ST90R50—3 multifunction timers, watchdog timer, serial peripheral interface, 2 serial communications interfaces, 2 I/O ports driven by DMA/timer, 8-bit ADC, 24-bit paged MMU, 9 I/O ports, 84-pin PLCC.

ST9054—32 kbytes ROM/EPROM/OTP memory, 1.2 kbytes RAM, 3 multifunction timers, watchdog timer, serial peripheral interface, 2 serial communications interfaces with DMA, 8-bit ADC, 24-bit paged MMU, 9 I/O ports, 84-pin PLCC.

SUPPORT

□ **HARDWARE** SGS-Thomson offers an ST9 ICE that uses a PC as the front end. The PC runs a symbolic debugger linked to the target μC. An evaluation board is also available with a ROMless ST9 and onboard programmable memory. An EPROM programming board programs ST9s.

□ **SOFTWARE** ST9 software-development tools include a macroassembler, C compiler, linker/loader, library archive to maintain software object files, and software simulator. The assembler provides high-level-language construct macros to simplify assembler coding. These constructs include if, while, do, loop, switch, and break. A real-time operating-system kernel is also available.

Texas Instruments TMS370

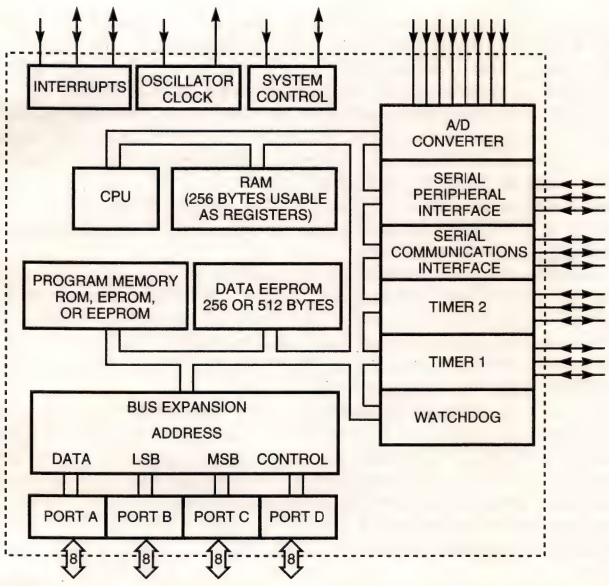
- Reg oriented; 128 regs in RAM
- 73 instr
- 2 to 32 kbytes ROM/EPROM
- 256 to 512 bytes EEPROM
- 128 bytes to 1 kbyte RAM
- Privileged mode
- Nonmultiplexed ext bus; 15-bit addr, 8-bit data
- 2 16-bit timers; watchdog timer
- 3 ext intr, 29 total intr
- Up to 55 I/O pins
- 2- to 20-MHz ext clock (divide-by-4 internal)
- 200-nsec NOP, reg-reg ADD
- 9-μsec MPY; 11-μsec DIV
- 32.8-μsec 8-bit A/D conversion
- 400-nsec memory R/W
- 95 μA max
- 4-μsec intr latency

□ OVERVIEW Texas Instruments' TMS370 family of 8-bit μCs handles low- to mid-range applications in the automotive, industrial, communications, and security industries. Developed in the mid 80s, the TMS370's register-based architecture has up to 256 registers and 32 kbytes of program ROM. Some variations have up to 512 bytes of on-chip data EEPROM, and one TMS370 version has 32 kbytes of program EPROM for program and system development. Clock rates go up to 20 MHz, which delivers a 1.6-μsec register-register ADD. Among the peripherals are a timing subsystem that includes capture/compare registers, two sets of 16-bit timers, an 8-bit ADC, and two serial-communications-port options. OTP versions are available for prototyping or debugging.

□ VENDORS/PRICING Texas Instruments developed the TMS370 and is the sole source.

370C311 (2 kbytes ROM, 128 bytes RAM, serial peripheral interface, timer, 22 I/Os, 28-pin DIP), $1.25. 370C056 (16 kbytes ROM, 512 bytes EEPROM, 512 bytes RAM, serial peripheral interface, serial communications interface, timer, ADC, 55 I/Os, 68-pin PLCC), $8.85. 370C342 (8 kbytes ROM, 256 bytes RAM, serial communications interface, 2 timers, ADC, 36 I/Os, 44-pin PLCC), $4.25.

ARCHITECTURE



The TMS370 is a second-generation, register-based architecture. It relies on a base of up to 256 registers in a RAM register file. The CPU can address these registers as registers or as RAM. RAM ranges from 128 bytes to 1 kbyte. As much as 512 bytes of on-chip EEPROM can be added for nonvolatile storage of constants or critical data.

The processor stack is in the register RAM and referenced by an 8-bit stack pointer. Instead of being memory mapped, the on-chip peripherals are register-file mapped: Each peripheral is assigned a frame of 16 registers in a peripheral file—an equivalent to the register file in the addresses space. The peripheral file has 16 frames, one of which holds the system and EEPROM/EPROM control registers.

Instructions range from basic operations to 2-address operations, such as adding data using a register and returning the results to the register. The CPU has some 16-bit operations, such as word moves (2 registers) and incrementing a word, and uses 16-bit offsets for jumps and register pairs as an address. All arithmetic, however, is 8 bit.

Instructions take a variable number of cycles. Each cycle is a quarter of the external clock cycle, or 200 nsec for a 20-MHz clock. Instruction cycles range from 8 for an accumulator-to-register ADD to 21 cycles for a word move.

The TMS370 addresses up to 112 kbytes of external memory. The nonmultiplexed external bus provides 15 address bits and 8 data bits. The μC has up to 6 programmable chip selects for memory banking. External memory can be RAM or ROM. To run at 20 MHz with no wait states, the controller needs a 200-nsec-cycle memory. Wait states are programmable for memory or I/O.

Stack—In reg-file RAM, restricted to 128 or 256 bytes with 8-bit SP. PUSH and POP instr move data between reg and stack.

Addressing modes—Two types: general, which has an 8-bit addressing range, and extended, which uses a 16-bit range. General modes include implied, reg, peripheral (peripheral file), immediate, PC relative, and SP relative. Extended has 2 basic subsets: absolute and relative. Each has direct, indexed, offset-indirect modes. Indirect provides a way to walk through memory using reg arithmetic.

Bit operations—Include jump if bit is 0 or 1, complement, set or clear bit. Instr operate on regs in reg or peripheral file.

Special instructions—Increment and decrement (can increment words), 1's or 2's complement, double-byte move for reg pairs and memory, swap nibbles and decimal add for BCD arithmetic, compare and exchange regs. Can decrement source and jump if not 0 and check 2 sources and jump if there is at least one matching bit in each or at least 1 nonmatching bit pair.

□ PERIPHERALS

EEPROM—Programmable, on-chip (5V), part of data memory. 256 or 512 bytes organized in erasable 32-byte blocks with block-level write protection. Also, 4 kbytes EEPROM program memory for prototyping.

Timers—Timer 1 contains 16-bit counter, 16-bit watchdog timer, 8-bit prescalar counter, 2 compare/capture regs with PWM output toggle. Timer 2 has all but watchdog. Both can do input capture and output compares on their counters and PWM signal generation.

Serial communications ports—Serial communications interface for asynchronous links with NRZ format and double-buffered transmitter/receiver. Serial peripheral interface for synchronous links; handles packets up to 8 bits, links to μC or peripherals.

ADC—8-channel input; 32.8-μsec conversion time, 1-μsec settling time. Conversion takes 18 cycles.

Programmable acquisition and control timer—RAM-based module uses 128 bytes dual-ported RAM to hold regs. Has 20-bit timer/counter, 8-bit event counter, input capture on 6 pins, output compare, and 8 PWM signals.

Reset/halt signal—Provides hardware indicator of chip state. After resetting μC, signal goes low if chip is in standby mode.

Mode	Current (max)	Voltage (V)	Clock (MHz)
Run	56 mA	5	20
Run	11 mA	5	2
Standby	28 mA	5	20
Halt	100 μA	5	0

In 64-pin DIP, 68-pin PLCC.

SUPPORT

□ HARDWARE TI's TMS370 development systems range from a simple evaluation kit to an ICE and debugger. ICEs are also available from third-party vendors as are EEPROM/EPROM and gang EPROM programmers.

□ SOFTWARE Assemblers, linkers, and C compilers are available for the TMS370 from TI and third-party vendors. TI's C compiler comes with a source-code debugger. A third-party instruction-set simulator that runs on a PC is also available.

□ **OVERVIEW** Toshiba's TLCS-90 8-bit μC combines the Z80's adaptable instruction set with a batch of embedded peripherals. The controller sports a Z80-like dual set of eight 8-bit general registers. Its peripherals include 8- and 16-bit timers; a 4- or 6-channel ADC; a 2-channel, 8-bit DAC; a SYNC/ASYNC serial port, up to 54 I/Os, a dual-channel stepping-motor-controller port, and a watchdog timer. Toshiba engineers added a DMA controller that processes internal interrupts directly without involving the CPU. The TLCS uses clock-stealing DMA to move data, offloading the CPU. Used mainly in Asia for embedded-control tasks ranging from industrial control to appliances and commercial goods, the TLCS-90 is now being marketed in the US. Toshiba plans to extend the architecture to build both 16- and 32-bit μCs.

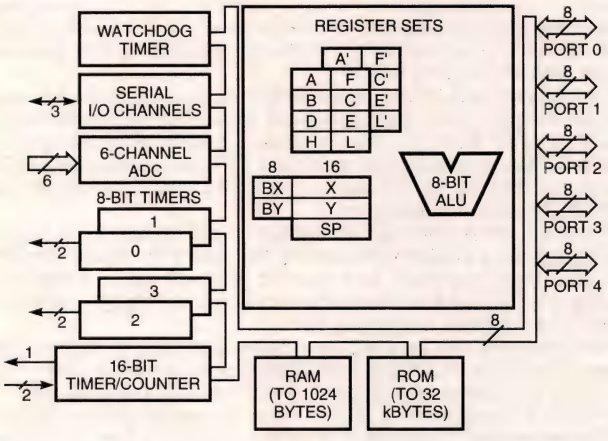
□ **VENDORS/PRICING** Toshiba is the developer and sole supplier of TLCS-90 μCs.

TMP90C840 (8 kbytes ROM/ROMless), $6.55/$9.05; TMP91C640 (16 kbytes ROM/ROMless), $6.95/$9.55; TMP90C400 (4 kbytes ROM), $6; TMP90CM40 (32 kbytes ROM), $9 (10,000); TMP91C640 (16 kbytes EPROM/OTP), $79.50/$29.50 (1000).

Toshiba TLCS-90

- 2 sets of 8 8-bit regs
- 2 index, 1 stack 16-bit regs
- 163 instr
- 4 to 32 kbytes ROM
- 128 bytes to 1 kbyte RAM
- 64-kbyte shared addr space for up to 1 Mbyte data
- Multiplexed/nonmultiplexed bus: 16-bit addr, 8-bit data
- MMU extends data space to 8 Mbytes
- 4 8-bit timers, 1 16-bit multifunctional timer
- Watchdog timer
- DMA controller
- 28 to 54 I/O pins
- 4 ext intr
- 16-MHz ext clock (divide-by-2 internal)
- 500-nsec reg-reg ADD
- 250-nsec NOP
- 2.0-μsec MPY, DIV
- 2-internal-clock mem R/W
- Up to 2 memory wait states
- 1.75/6.0-μsec/byte DMA; 256-byte block max
- 11.87-μsec A/D conversion
- 2.4-μsec intr latency
- Some 3V parts

ARCHITECTURE



Toshiba's TLCS-90 is the basic Z80 instruction set embedded in an 8-bit μC. Unlike the Z80, which is a μP, the TLCS-90 can execute code from on-chip ROM, and on-chip RAM provides local, dynamic storage. Timers, PWMs, and other on-chip peripherals link the core CPU to the external world.

Like the Z80, the TLCS-90 μC relies on a core set of general-purpose registers. These eight 8-bit registers are A, B, C, D, E, F, H, and L. The registers can be paired for 16-bit loads, stores, and arithmetic operations. The TLCS-90 also has an alternate register set: A', B', C', D', E', F', H', and L'. Programs can exchange the alternate registers with registers from the core set for fast context switching and register storage. However, the CPU cannot operate on the alternate register set directly.

Supplementing the general-purpose registers are two 16-bit index registers: the stack pointer and program counter. The 16-bit index registers—as well as 16-bit loads, exchanges, and arithmetic operations—make 16-bit addressing easy. Two 8-bit bank registers extend addressing from 16 to 24 bits, and an MMU extends addressing to 8 Mbytes of data. However, extended addressing is not available on all TLCS-90 μCs.

A pseudo-pipeline speeds operations. The TLCS-90 CPU has two stages: In the first stage, the CPU fetches and decodes instructions; in the second stage, the decoded instructions are executed. While the current instruction executes, the CPU fetches and decodes the next one. Instructions have 1 or 2 op-code bytes. Immediate and address data can take up to 3 bytes; the maximum instruction length is 5 bytes (2 op-code, 3 data bytes). The first op-code byte specifies the position of the second op-code byte in the instruction stream.

The μC usually has a synchronous external bus, but some chips have no external bus and execute from on-chip memory only. Both multiplexed and nonmultiplexed bus versions are available. Some chips also have wait-state registers that can generate up to 2 wait states for interfacing to slower memory. A standard memory cycle takes 4 external clocks.

An on-chip DMA controller can directly offload interrupt processing from the CPU. TLCS-90 DMA controllers handle 4 to 11 DMA channels, each programmed for a specific interrupt event. An event interrupts the CPU but does not require a context switch. Instead, the DMA hardware itself can move a data block, byte by byte, from one memory location to another. Memory blocks can be up to 256 bytes. The two types of TLCS-90 DMA controllers are the slower, more general μDMA and the faster HDMA, which handles 2-byte transfers.

Addressing modes—Reg, immediate, reg indirect, index, reg index, extended, direct, relative, extended data area (above 64 kbytes).

Special instructions—Exchange with alternate reg set; exchange regs, load increment/decrement and repeat; increment/decrement; decrement and jump if not zero; increment/decrement word, compare, increment/decrement and repeat; push and pop; load data block (mem to mem); search data block (search up to 64 kbytes for a pattern with 1 instr).

Bit instructions—Bit test, set bit, reset bit, test and set.

□ VARIATIONS

TMP90C840/1—8 kbytes ROM/ROMless; 256 bytes RAM; 6-channel, 8-bit ADC; serial I/O; 4 8-bit timers; 1 16-bit timer; watchdog; 2-channel stepping-motor control; 11 DMA channels; 4 ext intr; 54/38 I/Os; 64-pin DIP/QFP.

TMP9xC640—16 kbytes ROM/EEPROM/OTP memory; 512 bytes RAM; 6-channel, 8-bit ADC; serial I/O; 4 8-bit timers; 1 16-bit timer; watchdog; 2-channel stepping-motor control; 11 DMA channels; 4 ext intr; 64-pin DIP/QFP.

TMP90C400—4 kbytes ROM, 128 bytes RAM, serial I/O, 4 8-bit timers, 1-channel stepping-motor control, 8 DMA channels, 3 ext intr, 5 8-bit ports, 64-pin DIP/QFP.

TMP90CM40—32 kbytes ROM; 1 kbyte RAM; 6-channel, 8-bit ADC; serial I/O; 4 8-bit timers; 1 16-bit timer; watchdog; 2-channel stepping-motor control; 11 DMA channels; 4 ext intr; 64-pin DIP/QFP.

TMP90C802—8 kbytes ROM, 128 bytes RAM, 4 8-bit timers, 1-channel stepping-motor control, 4 DMA channels, 32 I/Os, 40-pin DIP/SOP.

TMP90C051—8-Mbyte addr space, MMU, 8 ext intr, 2 serial I/O channels, 4 8-bit timers, watchdog, 2-channel stepping-motor control, 2 high-speed DMA channels, 12 DMA channels, 31 I/Os, 80-pin QFP.

TMP90C844

Mode	Current (max at 5V)	Clock (MHz)
Run	50 mA	16
Idle	5 mA	16
Stop	40 μA	0

In 64-pin DIP/QFP.

SUPPORT

□ **HARDWARE** Toshiba sells evaluation boards and an ICE for all TLCS-90 chips.

□ **SOFTWARE** Toshiba supplies a macroassembler/linker, C compiler, and source-level debugger.

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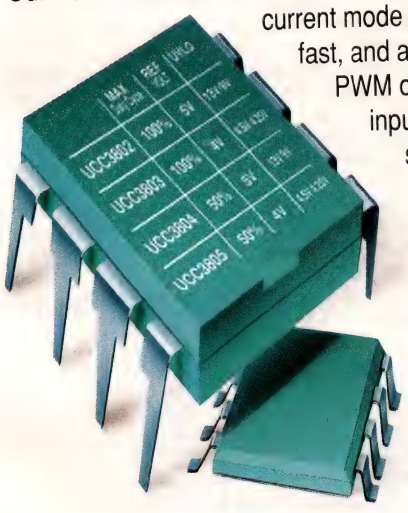

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CIRCLE NO. 52

□ OVERVIEW

The 8-bit Z8 handles embedded applications ranging from low-end products such as mice controllers to high-end ones like disk-drive and servo control. Z8 family members range from a minimal 18-pin DIP μC to a Z8 CPU integrated with a 16-bit DSP processor. Z8s don't have classical on-chip RAM but instead use a small number of register sets for on-chip dynamic storage. The Z8 does, however, access external memory for both code and data.

□ VENDORS/PRICING

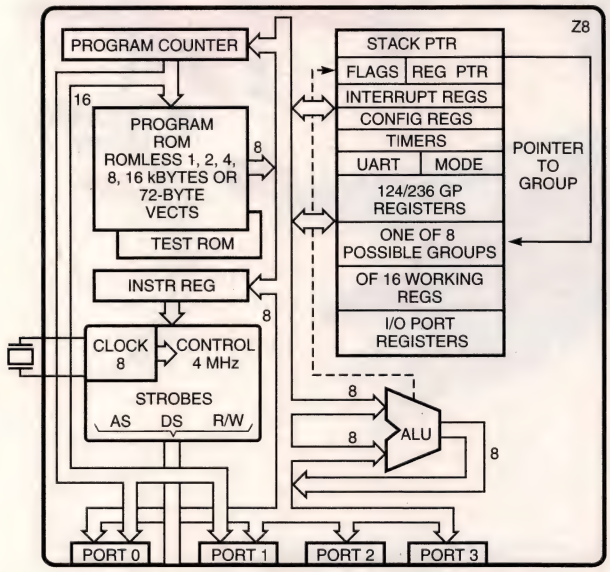
Zilog developed and sells the Z8. Second-source vendors include SGS Thomson, VLSI Technology, and Sharp. SGS's ST9 is a variant of the Z8. Zilog's Z8s have the designation Z86Cxx.

Z89120 (10 MHz, 4 kbytes RAM, 24 kbytes ROM, 68-pin PLCC), $11.25. Z86C95 (20 MHz, 256 bytes RAM, 80-pin QFP), $12.95 (1000). Z86C93 (25 MHz, 256 bytes RAM, 44-pin PLCC), $6.70 (1000). Z86C40 (12 MHz, 256 bytes RAM, 4 kbytes ROM, 40-pin PLCC, $2.42 (15,000).

Zilog Z8

- 124 to 256 8-bit regs in groups
- 46 pipelined instr
- 144 to 256 bytes RAM (regs, I/O ports, SP)
- 2 to 20 kbytes ROM/OTP memory
- 2 64-kbyte addr spaces for code and data; data ext only
- 6 addr modes
- 16-bit DSP coprocessor
- 4 ext, 2 internal intr
- Up to 56 I/O pins
- 4/12/16/20-MHz clock (divide-by-2 internal)
- 4-stage pipeline
- 100-nsec ADD, NOP (16 MHz)
- 1-cycle 16-bit MPY, MPY and accumulate with DSP
- No MPY or DIV instr
- 6 internal clocks for ext-memory access
- 1-μsec intr response time at 16 MHz

ARCHITECTURE



The Z8 is a stripped-down μC initially aimed at mid- to low-end applications. Zilog has since beefed it up by adding DSP muscle for math processing. The Z8 architecture is unusual—it has 3 address spaces: 64 kbytes code, 64 kbytes data, and a CPU register file with up to 256 registers. The external code and data spaces can be combined off chip. References to external memory are only loads or stores; data manipulation is confined to operations between on-chip registers. Switching between register groups or sets delivers a fast context switch.

The Z8's core is a simple register-file-based architecture with 124 to 256 8-bit registers in SRAM. The SRAM also holds the I/O control registers, 16-bit stack pointer (2 registers), and register pointer. On-chip program memory runs from 2 kbytes to 20 kbytes of ROM or OTP memory.

Z8s have complex instructions, which helps minimize coding multiple operations such as fetching data, operating on it, and incrementing address pointers. Basic Z8s have no hardware multiply or divide instructions, however, Zilog has added a MPY/DIV unit to some versions.

For heavyweight math processing, Zilog added a 16-bit DSP MAC (multiply and accumulate) coprocessor that has its own register file and RAM. In the latest Z8 chip—the 86120—the CPU and the DSP coprocessor operate independently. The processors communicate via shared register memory and interrupts. On the 86120, the DSP coprocessor controls its own I/O peripherals including ADCs and DACs. The coprocessor can take analog data in, operate on it, and output it without affecting the Z8 CPU, which runs from its own memory.

The DSP MAC coprocessors are 16-bit processors with their own local program and data memory to hold parameters and results. They can do a multiply-accumulate cycle while updating the addressing for the next set of X, Y parameters needed for the next MAC cycle.

Block transfers—Load-external-data-and-autoincrement instr speeds loading data from memory by moving a byte from memory to reg and incrementing memory and reg addr held in working regs. Load-constant-autoincrement instr does the same thing for moving constants from program memory to reg file. Both save time and code by automatically indexing addr pointers.

16-bit operations—CPU addresses up to 64 kbytes, which requires a 16-bit addr. CPU provides 16-bit increment and decrement operations to reg pairs to ease addressing. SP stack operations reference on-chip RAM (8-bit addr) or ext data memory (16-bit addr).

Special operations—Loop instr (decrement and jump if not 0), reg increment and decrement, and BCD arithmetic.

□ PERIPHERALS

Timers—Two 8-bit timers with prescalar.

Watchdog timer—Programmable to 5-, 15-, 25-, or 100-msec periods. One-shot timer starts execution power-on.

MPY/DIV unit (Z86C95)—16-bit, hardwired MPY, DIV.

DSP MAC coprocessor—Has 16×16-bit multiplier and 24-bit ALU and accumulator. It has two 256 16-bit-word RAMs (X, Y values) and 512 bytes to 8 kbytes code memory (RAM or ROM, depending on chip version).

Disk controller (Z86C99)—Integrates Z8 CPU with DSP processor and hardware for disk control and interfacing.

18-pin-DIP versions—1 to 2 kbytes ROM, 124 bytes RAM, 14 I/O pins.

Z86C62

Mode	Current (max)	Voltage (V)	Clock (MHz)
Normal	150 mA	5	20
Halt	25 μA	5	20
Stop	10 μA	5	0

In 64-pin DIP, 68-pin PLCC.

SUPPORT

□ **HARDWARE** Evaluation boards are available from Zilog for most Z8 μCs, as are evaluation boards for specific applications such as keyboards, IR control, and modems. Zilog has ROMless and piggyback versions for development and prototyping. ICEs and programmers are also available for most chips.

□ **SOFTWARE** Development software enables terminal- or PC-based debugging with a ROM monitor from Zilog. Zilog also supplies a terminal emulator with a ROM monitor and a macroassembler/linker/loader.

□ OVERVIEW

The Z80 is one of the pioneering 8-bit μPs. Ex-Intel engineers based the Z80 on the 8080 and added a dual-register-set architecture with index registers, built-in memory refresh, and a more powerful, extended instruction set. Used in early personal computers, the Z80 family also has a solid embedded-systems base in communications (modems and Appletalk), disk controllers, and various monitor/control systems. Later versions such as the Hitachi 64HD180 and Zilog Z80180 have extended addressing (to 1 Mbyte) and specialized on-chip peripheral controllers for communications.

□ VENDORS/PRICING

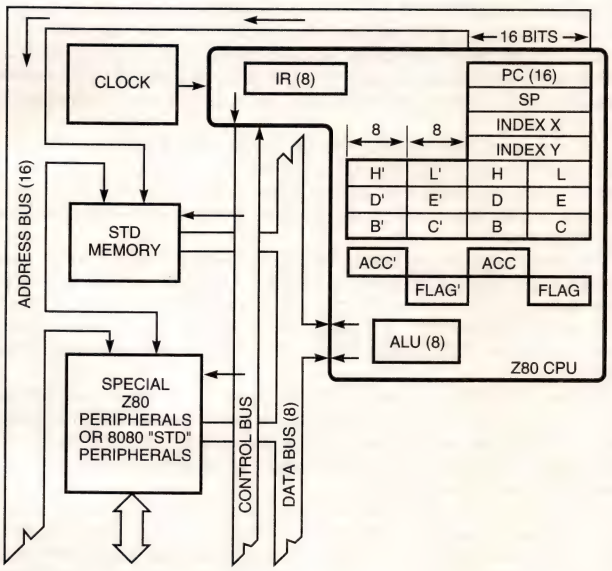
Zilog is the original Z80 family vendor. Z80 (designated Z84xxx by Zilog) second sources include Toshiba, Hitachi, SGS Thomson, NEC, Sharp, and VLSI Technology. Zilog, Hitachi, and Toshiba use the Z80 as an ASIC core. Hitachi, in a joint development with Zilog, designed the 64180—a Z80 with an MMU that extends addressing to 1 Mbyte. Zilog and Hitachi offer several 64180-based μPs with on-chip memory.

Pricing for the base Z80 is down to $1 or less in high volume. Z84C01, $2; Z80182, $15; Z80180, $5; 64180, $5.75 to $7.25.

Zilog Z80

- 2 sets of 8 8-bit regs
- 16-bit special regs: SP, PC, 2 index
- Unified 64-kbyte addr space; off-chip memory
- 16-bit addr, 8-bit data nonmultiplexed ext bus
- Complex instruction set with DMA
- MMU adds 1-Mbyte addr space (64180, Z80180)
- 2 16-bit timers, 2 DMA channels, 2 UARTs, 2 serial ports (Hitachi Z80180)
- DC to 20 MHz for CMOS μC
- Static CMOS versions have divide-by-1 internal clock; NMOS has divide-by-2 clock
- 3 (static core) or 4 (NMOS core) clocks/cycle
- 300-nsec ADD; 150-nsec NOP
- 17-clock MPY, DIV
- 150-nsec, 3-cycle memory R/W
- 19-cycle intr latency at 20 MHz (Z84C50)

ARCHITECTURE



Introduced in 1977, the Z80 is still a favorite for many design engineers. It is an extended 8080 with a complex set of 158 instructions. The Z80 family relies on off-chip memory—with one exception, the Z84C50, with 2 kbytes of SRAM. In the 8-bit world, the Z80 is ideal for large-scale memory-to-memory operations.

Two banks of 8-bit general-purpose registers make for fast context switches. But even with two register sets, the Z80 is an accumulator-based CPU. All 8-bit arithmetic/logical operations use the accumulator (current A register) as one source and the destination. Compare operations also are relative to the accumulator register.

Sixteen-bit special registers make addressing much easier for programmers. These registers include 2 index registers, a stack pointer, and a program counter. Two special registers also help coding: the interrupt register, which holds the 7 upper address bits for interrupt vectors, and the 7-bit memory-refresh register, which uses the lower address bits for memory refresh.

The Z80's complex instruction set provides many programming options, including block memory moves and character memory searches. Instructions are 1, 2, 3, or 4 bytes long. To simplify addressing, the CPU does 16-bit accesses (2 8-bit words accessed sequentially).

A new, static Z80 core is replacing the older core. Not only is the static core faster, but it lets designers control power consumption by drastically dropping the clock rate. The new core runs at the oscillator clock rate; the older core runs at half that rate. The Z80 easily handles complex communications timing sequences—especially the Z80180 family, which has specialized communications peripherals. These peripherals include two DMA channels, two UARTs, one or two serial communications controllers, and a counter/timer circuit.

16-bit arithmetic—Add, subtract, increment, or decrement reg pairs.

Block transfer and search—Move up to 256 bytes in block transfer using reg-pair addressing. Can search a block for a character.

Bit operations—Set, reset, test a bit in reg or memory location.

Special operations—Reg increment and decrement instr minimizes counter operations. BCD arithmetic for accumulator operations: add, add with carry, subtract with carry, increment, decrement, and negation.

□ PERIPHERALS/INTERFACES

Wait-state generator—Programmable, as in the Z80182.

MMU—Maps addr from 64-kbyte local segment to 1-Mbyte global memory. On-chip Z80180 and Hitachi 64180.

DMA channels—Allow movement of up to 64-kbyte data blocks between I/O and memory or memory and memory; 3 modes: request, burst, cycle steal.

Power down—Detects brownout conditions and triggers reset intr condition.

Counter/timer unit—4 independent program counter/timer channels. Available as separate chip or integrated with Z84 or Z80180 families.

Serial and parallel I/O controllers—Available on-chip or as support chips. Handle parity generation/checking, frame checks, frame-error recovery. Serial I/O controller has 2 independent, full-duplex serial channels for asynchronous or synchronous protocols with CRC and parity generation. Supports polling, vectored or nonvectored intr.

Extended serial communications controller, PC interface—On-chip Z85230; has 2 serial and 2 DMA channels. Handles common synchronous and asynchronous protocols; interfaces to PC XT/AT bus.

Z80S180 communications controller

Mode	Current (max)	Voltage (V)	Clock (MHz)
Normal	150 mA	5	20
Sleep	25 μA	5	20
Standby	10 μA	5	0

Z84xxx in 40-pin DIP, 44-pin QFP, or chip carriers; Z80182 in 100-pin QFP; Hitachi 64180x in 80-pin QFP.

SUPPORT

□ **HARDWARE** Support chips for the basic Z80 CPU include controllers for the counter/timer, DMA, parallel I/O, serial I/O, serial communications, and enhanced serial communications controllers. Many of these chips are with the Z80 core for high-integration chips such as the Z80182. Zilog has evaluation boards and ICEs for most family members.

□ **SOFTWARE** The Z80 has 15 years worth of software tools including assemblers, Forth and Basic interpreters, and C compilers. Zilog offers the Electronic Programmers Manual, an on-line reference and interactive-programming aid for peripherals.

Hitachi H8/300/500

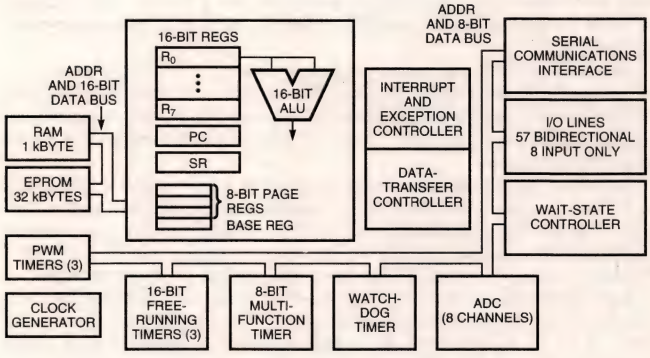
- μC family: 8/16-bit H8/300, 16-bit H8/500
- 3xx has 16-bit ALU, 8/16-bit regs, 16-bit instr word
- 5xx has 16-bit ALU, regs; multibyte instr
- Reg-oriented, 8 general-purpose regs
- 3xx: up to 1 kbyte RAM, 32 kbytes ROM
- 5xx: up to 2 kbytes RAM, 62 kbytes ROM
- 64-kbyte/16-Mbyte addr space (3xx/5xx)
- 52/63 instr (3xx/5xx)
- Up to 9 ext intr
- Up to 58/57 I/O pins
- 12/16/20/25-MHz clock (divide-by-2 internal)
- 200-nsec instr cycle, NOP, ADD (3xx)
- 160-nsec instr cycle, NOP, ADD (5xx)
- 1.4-μsec MPY, DIV (3xx); 1.84-μsec MPY, DIV (5xx)
- 3-clock ext-mem R/W; 2-clock internal-mem R/W
- 12.25-μsec 8-bit ADC; 13.8-μsec 10-bit ADC
- 2.90/5.60-μsec max intr latency (3xx/5xx)

□ OVERVIEW Introduced in 1987, Hitachi's H8 series of 8-bit μCs is aimed at mid- to high-end embedded applications in the automotive, office-automation, and communications industries. Register-based, the H8 includes two lines: the H8/300, an 8-bit μC with 16-bit instruction words, and the H8/500, a 16-bit μC with multibyte instruction words. The H8/500 was introduced in 1988 but withdrawn from the US because of a lawsuit with Motorola over the 68030. The μC was reintroduced in 1992. Both controllers sport complex timers with compare/capture registers and PWM generators and have low-power 3V versions. Both lines also have a full set of peripherals, and the H8/500 has up to 62 kbytes of EPROM/ROM and a data-transfer service for processing interrupt events. The H8/570, introduced in 1992, adds a 64-bit, EPROM-based I/O subprocessor for tailored timing and I/O functions.

□ VENDORS/PRICING Hitachi is the developer and sole source of H8 μCs.

The following chips have ROM and come in QFPs, except where noted: H8/520, $9.40; H8/532, $11.25; H8/536, $17.45; H8/570, $29.25 (OTP memory); H8/322, $5.40; H8/3101, $7 (1,000,000, in SOP); H8/330, $7.

ARCHITECTURE



The register-based H8 has 8 general-purpose registers supplemented by a PC, PSW, and address-paging registers. The architecture resembles that of larger, RISC-like processors in that the registers are not part of a register-banking or third-addressing-space scheme. And like many higher-end CPUs, the H8's instruction set is orthogonal, making the chip a good base for high-level languages like C.

Two processor lines make up the H8 family: the H8/300 and H8/500. These lines represent two different implementation philosophies but share a common instruction base and register-based architecture. The two lines are not code compatible, but they use the same mnemonics and basic addressing philosophy.

The initial H8 implementation, the H8/300, is an 8-bit μC with a 16-bit ALU and an 8-bit external-memory interface. The CPU sees the registers as either 8 or 16 bits, the internal data/instruction path is 16 bits, and instructions use a 16-bit word (2 or 4 bytes, depending on supplemental addressing data). The H8/300 handles 16-bit arithmetic, thus making address manipulation easy.

The later H8/500 is a true 16-bit μC. It has a 16-bit ALU and data path and 16-bit registers. The CPU references registers as a set of 8 16-bit registers or 16 8-bit registers. The external data path is 8 or 16 bits wide and is dynamically resizable. The chip addresses a 16-Mbyte space and has a programmable wait-state generator.

The H8/300 has a RISC-like implementation: The controller has a fixed instruction word (with a supplemental word for additional data) and a load/store architecture. As with RISC processors, all data manipulation takes place between registers—all memory instructions are simple loads and stores.

The H8/500 has a different implementation. Operations are not restricted to registers, and instructions have variable byte lengths. For many instructions, the CPU fetches the 1- to 3-byte effective-address modifiers first, before the actual op code. This fetching order lets address generation proceed in parallel with instruction decoding (from the following op-code bytes). The H8/500 has a 3-byte instruction-prefetch queue—the CPU fetches the next instructions (PC relative) while processing the current one.

Both CPUs have a single, unified address space. The H8/300 has a 64-kbyte address space; the H8/500 has a 16-Mbyte space. The 500 uses a page-management scheme to extend addressing. The scheme involves using four 8-bit page registers to build effective addresses (code-, data-,extended-, and stack-page registers). The address space includes a hardware-supported stack in data RAM.

Addressing modes—Reg direct/indirect, reg indirect with fixed displacement, reg indirect with preincrement/decrement, immediate, absolute, PC relative. Both CPUs support indirection.

Special instructions—Increment/decrement reg, compare reg data, load/store multiple regs (500), link/unlink (500 for building user stack frames), test and skip (500).

Bit manipulation—Bit set/clear/complement/test. The 300 has 14 bit-manipulation instr.

Data-transfer controller—Offloads CPU during processing intr. Moves data between memory and I/O via DMA cycles.

□ VARIATIONS The H8/500 has 8 timers (3 16-bit), capture/compare regs, watchdog and 3 PWM timers, and data-transfer and memory-wait-state controllers. Most H8/300 μCs have 1 or 2 16-bit timers, 2 or 6 8-bit timer/counters, 6 or more compare/capture regs, and 1 or 2 PWM channels.

H8/520—16 kbytes ROM; 512 bytes RAM; 10-channel, 8-bit ADC; timer complex (3 16-bit timers); 1 serial channel, 47 I/Os, 64-pin DIP/QFP, 68-pin PLCC.

H8/532—32 kbytes ROM, 1 kbyte RAM, complex timer, 80-pin QFP, 84-pin PLCC.

H8/536—62 kbytes ROM; 2 kbytes RAM; timer complex; 10-channel, 8-bit ADC; 57 I/Os, 80-pin QFP.

H8/570—2 kbytes RAM; watchdog and 3 PWM timers; 8-channel, 10-bit ADC; 1 serial channel, I/O subprocessor (I/O controller with 512×64-bit EEPROM program block), 66 I/Os, 112-pin QFP.

H8/322—8 kbytes ROM, 256 bytes RAM, 8-/16-bit timers with capture/compare/PWM, 47 I/Os, 2 serial ports, 4 ext intr, 64-bit DIP/QFP.

H8/330—16 kbytes ROM; 512 bytes RAM; 8/16-bit complex timers; 1 serial channel; 8-channel, 8-bit ADC; 58 I/Os; 80-pin QFP.

H8/3101—5 MHz, 10 kbytes ROM, 256 bytes RAM, 8 kbytes EEPROM with security functions, 1 I/O, 10-pin SOP. For smart cards and security applications.

H8 322/520

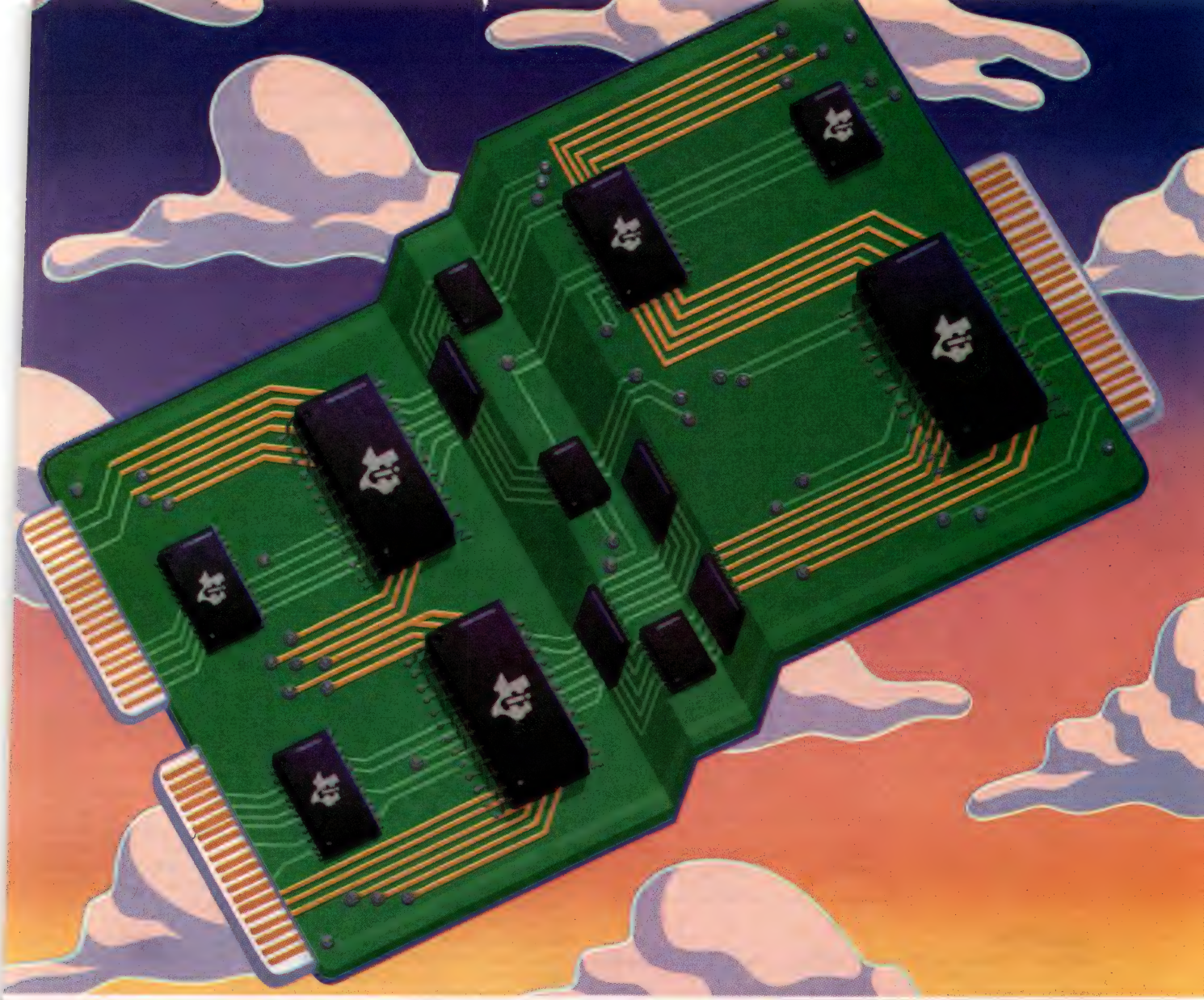
Mode	Current (max, 322/520)	Voltage (V)	Clock (MHz)
Normal	40/50 mA	5.5	10
Sleep	25/30 μA	5.5	10
Standby	5/20 μA	5.5	0

H8/322 in 64-pin QFP/DIP; H8/520 64-pin QFP.

SUPPORT

□ HARDWARE Hitachi and third-party vendors supply evaluation boards and ICEs. You can program OTP versions using EPROM programmers that handle Hitachi 256-bit EPROMs.

□ SOFTWARE Software tools for the H8 include cross-assembler/linkers, C compilers, C development environments, and a Forth system. Additionally, Togai InfraLogic (Irvine, CA) has a fuzzy-logic compiler for the H8, and real-time kernels are also available.



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SN74LVT245 Highlights

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V_{cc} Range:	2.7 V-3.6 V
Drive:	-32/64 mA I_{oh}/I_{ol}
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Bus Hold:	Eliminates pull-up resistors

For more information

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TEXAS INSTRUMENTS

CIRCLE NO. 42

Intel 8086/80186

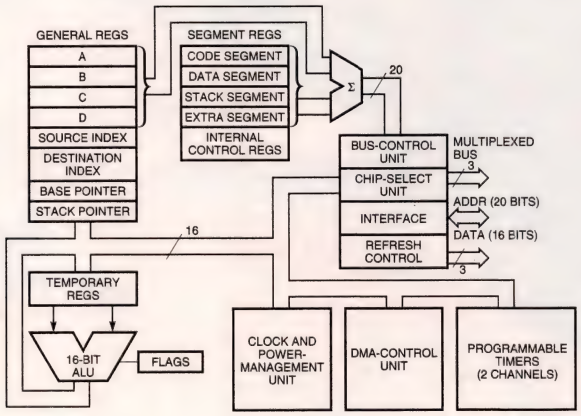
- 8806/88 core μP
- 80186/88 add peripherals
- 100+ instr (186 adds 10)
- 4 general, 4 index, 4 segment 16-bit regs
- 8- (8088) or 16-bit ext bus, multiplexed
- 1-Mbyte addr space—20 bits with segment regs
- 80187 floating-point coprocessor
- DMA, serial I/O channels
- Memory controller—chip select, wait states, refresh
- Up to 24 I/O pins, 8 ext intr
- Up to 40-MHz clock (20-MHz internal)
- 250-nsec reg-reg ADD, 625-nsec mem-reg ADD (at 32 MHz)
- 2.31-μsec MPY, DIV
- 3-internal-clock NOP
- 4-internal-clock mem R/W
- 5-Mbyte/sec DMA rate at 40 MHz
- 32-bit watchdog timer (186/188EC)
- 2.7, 5.5V parts
- 3.44-μsec intr latency

□ **OVERVIEW** Intel's 8086/88 is the μP that fueled the IBM PC's rise to dominate personal computers. Introduced in 1979, Intel engineers designed the chip to be code compatible with 8-bit 8080As. The 8086/88 debuted in 1979, and the 8088 8-bit-bus version powered the first PCs in 1981. The 8086 is a register-based architecture, but the registers are not all general purpose—there are dedicated segment and stack pointers. The 186/188 is an integrated chip for embedded systems. It includes memory chip selects, 3 timers, an interrupt controller, and 2 DMA channels. Some later 186/188 chips have programmable clocks or a CMOS core and can run from 2.7V to cut power; later 186s can interface to an 80187 math coprocessor. Chips & Technologies builds the F8680, a single-chip PC with an 8086 core.

□ **VENDORS/PRICING** Intel developed the 8086/8088; second sources include AMD, Matra, Fujitsu, Siemens, and Oki. 80186/188 second sources include AMD and Siemens.

These prices are for 100-unit quantities; clock rates are internal. 80C86A/80C88A (8 MHz, 40 pins), $11/$10; 80C186/188 (16 MHz, 68-pin PLCC), $10.05/$9.10; 80C186XL/188XL (16 MHz, 68-pin PLCC), $12.60/$11.70; 80C186/188EA (20 MHz, 68-pin PLCC), $14.40/$13.50; 80C186/188EB (16 MHz, 84-pin PLCC), $15.30/$14.40; 80C186EC (16 MHz, 100-pin QFP), $20.90/18.85; 80C1187EC(16 MHz, 44-pin PLCC) $123. Chips & Technologies F8680,$35.

ARCHITECTURE



Programmers and engineers have been throwing a lot of brickbats at the 8086 architecture, mainly because of its register organization and use of segmentation to simplify addressing. Yet, many programmers understand its architecture, and the 8086/88 has a huge base of development and applications software.

Actually the register-based 8086 architecture is fairly sophisticated and reflects that of the earlier 8080 and 8085 8-bit μPs. Operations center on fourteen 16-bit registers, which are organized into 4 general purpose, 4 pointer, 4 segment, and 2 special registers. The segment registers point to code, stack, local data, and external data segments. The CPU addresses each general-purpose register as 16-bit registers or two 8-bit registers.

The core architecture breaks down into two separate sets: the processor proper and the bus-interface unit, which asynchronously communicates to the outside world via a 8- or 16-bit, multiplexed system bus. The unit uses a 6-byte instruction prefetch queue to hold pending instructions. The bus-interface unit fills the queue each memory cycle unless it's reading or writing data.

The 8086/8088 and later 186/188s can run concurrently with an 80187 math coprocessor, or FPU. The FPU adds 68 operations including floating point and transcendentals. It has six 80-bit registers the CPU can access as either a stack or as discrete registers. The 187 shares the system bus; the CPU fetches both 186 and 187 instructions for execution. The CPU and FPU coordinate through ESCAPE and WAIT. The first puts memory data on the bus; the second halts the CPU until the FPU is done. The 187 uses three chip-select pins for handshaking.

All memory addressing is base relative, which makes developing embedded code because code is easily relocatable—just change the address base to relocate. The 186/188 bus supports multiprocessing. The local bus controller deploys a HOLD/HOLDA protocol that enables a CPU to take over the common system bus. The 186 memory controller supplies DRAM refresh signals as well as 10 to 13 memory chip selects to minimize memory glue logic. The 186/188 chips added two DMA channels.

Address segmentation—Lets CPU address up to 1-Mbyte space. 16-bit addr added to addr segment (segment reg shifted 4 bits left) to get 20-bit addr. Segments are 64 kbytes wide max.

Addressing modes—For code: program relative, direct, and indirect. For data: immediate, direct, direct-indexed, implied, base relative, and stack. Segment-pointer registers point to code, data, stack segments.

Special instructions—Exchange, increment, decrement, loop (decrements register, continues until 0), repeat prefix for repeating string operations (execute until zero or equal, or the reverse), and translate.

□ **VARIATIONS**

80C86A/8088—Basic 8086/88. 8 MHz, 3 timers, 2 DMA channels, 13 chip selects, 40-pin PLCC.

80C186/188—Basic CMOS version of 186/188. Up to 32 MHz, 3 timers, 13 chip selects, 2 DMA channels, 68-pin PLCC/PGA, 80-pin QFP.

80C186XL/188XL—Static core, up to 40 MHz, programmable internal-clock rate (div by 1/4/8/16), 2 DMA channels, 3 timers, programmable wait states (0 to 3), extended 68-lead PLCC/PGA.

80C186EA/188EA—Static core, 16 MHz (2.7, 5.5V), 2 DMA channels, 3 timers, intr controller, 13 programmable chip selects, 6 ext intr, 16 I/O pins, 68-pin PLCC/QFP.

80C186EB/188EB—Static core, 16 MHz (2.7, 5.5V), 2 8-bit I/O ports, 2 serial I/O ports with baud-rate generators.

80C186EC/188EC—Static core, up to 32 MHz, programmable internal-clock rate (div by 1/4/8/16/32), 4 DMA channels, 3 timers, watchdog timer, 10 chip selects, 22 I/O pins, 2 serial I/O ports with baud-rate generator, 8 ext intr, 100-pin QFP.

Chips & Technologies 8680—Static 8086-like core, up to 16 MHz, PC with timer, intr controller, DRAM controller, CGA graphics controller, DMA, keyboard interface, UART, supervisor mode, 160-pin QFP.

NEC V20/V30—Enhanced 8086-like chip, code compatible. Pipelined; additional instr, regs; 8/16-bit ext bus; 5/8/10 MHz; 40-pin DIP, 52-pin QFP, 44-pin PLCC.

NEC V25/V35—Single-chip microcomputer based on V20/V30. Up to 16 kbytes ROM, 512 bytes RAM (256 bytes as regs), 2 serial I/O ports, 3 timers, 24 I/Os, DMA and intr controllers, 8/16-bit ext bus (V35), 84-pin PLCC, 94-pin QFP.

80C186

Version, mode	Current (max)	Voltage (V)	Clock (MHz)
EC, normal	120 mA	5	32
EC, idle	85 μA	5	32
EC, power down	100 μA	5	0
EB, normal	50 mA	2.7	16
80C86, run	10 mA/MHz	5	to 8

EC in 100-pin QFT; XL in 68-pin PLCC, PGA; 80C86 in 40-pin QFP.

SUPPORT

□ **HARDWARE** A range of hardware tools is available for the 8086/88 and 80186/88 processors including ICEs, logic analyzers, evaluation boards, and third-party single-board computers. You can test code on PC development host before downloading to target system. However, there are some minor differences between the 80186 and the 8086.

□ **SOFTWARE** You can use both Microsoft and Borland compilers for cross development with software packages for writing embedded software and debugging it from a PC host. Compilers include C, C++, Fortran, Pascal, and PL/M; there are also Forth systems. Intel's free ApBuilder is an interactive, graphical programming environment for configuring and programming 186 peripherals.

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PLCC	20 SOIC	44 PLCC	68 PLCC	84 PLCC	100 PQFP
PQFP	16 SOIC	28 PLCC	44 PLCC	68 PLCC	84 PLCC
SOIC				44 PLCC	68 PLCC
					44 PLCC

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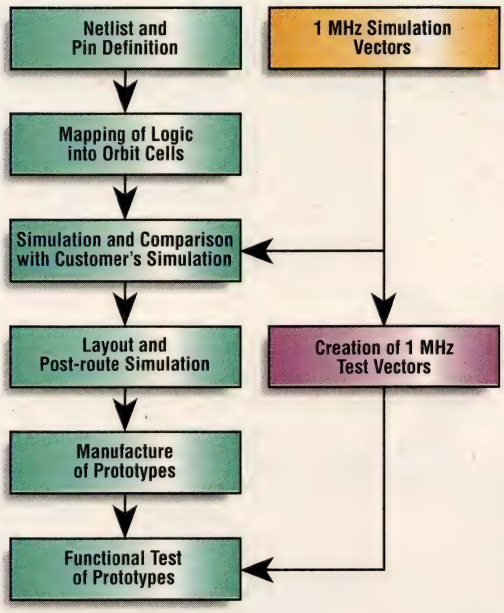

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•1 MHz simulation showing all pins in a print-on-change format

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CIRCLE NO. 43

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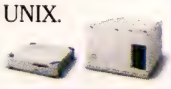

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CIRCLE NO. 44

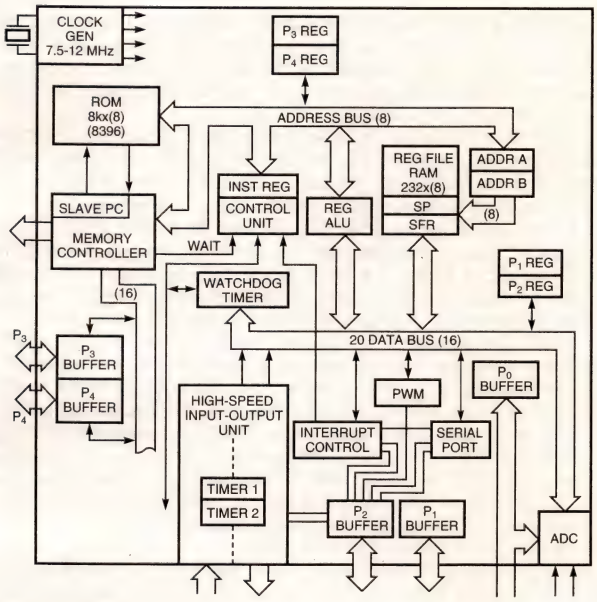
☐ **OVERVIEW** The Intel MCS-96 is the grand old man of 16-bit μCs. Originally developed as a custom processor for automotive applications, the MCS-96 has branched out into process-, industrial-, and motor-control applications. The register-based family's sophisticated peripherals include a PWM generator, high-speed timer/counter/compare unit, programmable ADC, and peripheral-event controller.

☐ **VENDORS/PRICING** Intel is the sole vendor.
80C198 (ROMless, 8-bit bus), $7.80; 83C196KB (8 kbytes ROM, 16-bit bus), $10.20; 83C196KC (16 kbytes ROM, 488 regs), $13.85; 87C196KD (32 kbytes OTP memory, 1000 regs), $24.80; 87C196KT (32 kbytes OTP memory, 1000 regs, 512 bytes RAM), $29.75; 87C196NT (32 kbytes OTP memory, 1000 regs, 512 bytes RAM, 1-Mbyte address space), $29.75.

Intel MCS-96

- Reg-based CPU, 232 general-purpose regs in banks
- Up to 1 kbyte RAM
- Up to 32 kbytes ROM/EPROM/OTP memory
- 64-kbyte or 1-Mbyte addr space
- Multiplexed ext bus, 8- or 16-bit data
- 2 16-bit timers; 16-bit watchdog timer
- Peripheral DMA controller
- Counter/timer unit and compare/capture regs
- Serial I/O
- Up to 56 I/O pins
- 12/16/20-MHz clock (divide-by-2 internal clock, CMOS; divide-by-3, NMOS)
- 400-nsec reg-reg ADD; 200-nsec NOP
- 1.4-μsec MPY; 2.4-μsec DIV
- 8/11-μsec A/D conversion (8/11-bit mode)
- 2-clock ext-memory R/W
- 4.3-μsec peripheral-transaction-service intr latency, 1.8- to 2.6-μsec execution
- 6.1-μsec intr latency

ARCHITECTURE



Intel's MCS-96, the first commercial 16-bit μC, is still going strong. Its surprisingly sophisticated architecture includes built-in register windows, advanced timer/counters, and a DMA-based peripheral-event handler that offloads interrupt service from the CPU. The architecture continues to evolve with higher silicon densities and advanced design techniques.

Unlike many early μCs, the MCS-96 is not accumulator based. Instead, the CPU is built around a set of on-chip RAM-based registers. Any of the 128 or 256 registers can function as a result accumulator. Temporary registers hold operand values during operations.

Some MCS-96 family members have on-chip RAM that can hold small critical, dynamic code or data and can implement register windowing. Register windowing can substitute a block in RAM for a block of registers. Accesses to a register in the window block are mapped to the windowed block in RAM. This technique makes fast context switches easy by shifting the register window to another block. Block sizes can be programmed for 16, 32, 64, or 128 bytes.

Instructions can have 1, 2, or 3 operands. Some instructions are more than 1 word. Register windowing helps minimize instruction size by letting 8 bits address a register in a movable window. I/O and special-function registers provide control and data points for chip peripherals. Horizontal windowing makes these registers accessible within a register window.

The MCS-96 has a 64-kbyte or 1-Mbyte address space that both code and data share. The address space works with both 8- and 16-bit external data buses. The external bus multiplexes data and address lines, so a buffer must hold the address stable during data transfers. The bus width can be changed dynamically. An on-chip memory controller lets the MCS-96 use a wide range of memory types and speeds. External-memory wait states are programmable.

Autoprogramming—CPU can program EPROM via 8-bit ext data interface.

Slave port—Some MCS-96s, such as the 196KR, have slave port for parallel communications with other CPUs. In slave-port operation, μC is slaved to a master CPU, which can write to or read from it.

Block moves—196KC/KB have block moves for nonoverlapping memory addr; 196KC's block-move instr is interruptible.

Special instructions—Indirect-autoincrement addressing; table-indirect-jump (196KC/KD/KR/NT) lets you jump via a table; decrement-and-jump-if-0; increment/decrement.

☐ PERIPHERALS/INTERFACES

Peripheral transaction service—Offloads CPU from intr processing; can handle up to 15 peripheral events. Execution operates on a cycle-stealing basis, interleaving operation with the CPU. On a peripheral event, the service moves data between the peripheral and memory.

ADC—8/10-bit successive-approximation ADC with 8 input channels. Sample-and-hold and conversion times are programmable.

Event processor array—Has two 16-bit timers, 10 capture/compare modules, event intr.

HOLD/HOLDA protocol—Lets processors share a common memory bus for multiprocessing.

Waveform generator—8xC196MC's waveform generator produces 3-phase sine waves for 3-phase motor control.

Mode	Current (166/167, max)	Voltage (V)	Clock (MHz)
Run	180 mA	5	40
Idle	20/25 mA	5	40
Power down	100 μA	2.5	0

166 in 100-pin QFP; 167 in 144-pin QFP.

SUPPORT

☐ **HARDWARE** ICEs and evaluation boards are available from Intel and other vendors. MCS-96-based single-board computers are available from third-party vendors for embedded applications. The 196KR lets you program the μC via the serial I/O port. A clock-out disable bit turns off clock output to reduce RFI.

☐ **SOFTWARE** The MCS-96 family has a range of development tools that includes assemblers and C and PL/M compilers. Also available from Intel is Apbuilder, a Windows-based interactive tool for programming MCS-96 peripherals. Apbuilder generates code, sets control registers, and activates peripherals. Intel also offers a package that translates 8051 code into MCS-96 code for moving applications to the 16-bit μC.

Mitsubishi 37700

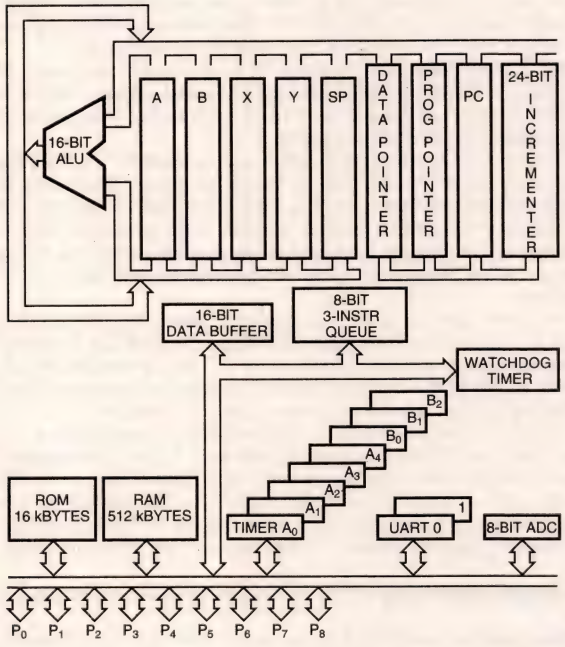
- 16-bit, 6502 superset
- 16-bit regs: 2 accum, 2 index, SP, PC
- 103 instr; 28 addr modes
- Up to 32 kbytes ROM/EPROM/OTP memory
- Up to 2 kbytes RAM
- Program-, data-bank regs extend addr
- Ext bus: 16/24-bit addr, 8/16-bit data
- 16-Mbyte addr space
- 8 16-bit timers, watchdog
- UART; 8-channel, 8-bit ADC
- Up to 68 I/O pins
- 3 ext intr
- 8/16/25-MHz ext clock (divide-by-2 internal)
- 2-clock min instr time
- 2-clock NOP, reg-reg ADD
- 25-clock MPY; 30-clock DIV
- 2-clock mem R/W
- 57-clock A/D conversion
- 4-mA max current (8 MHz, 3.3V)
- 2.7, 5.5V parts
- 127-clock intr latency

□ **OVERVIEW** Mitsubishi's 37700 family of 16-bit μCs is a superset of the 6502/6500 8-bit family. Mitsubishi fields the 6502-based 740 family in Japan, where the chip is one of the leading 8-bit μP/μCs. The 37700 builds on the basic 6502 instruction set and architecture. The accumulator-based CPU has two 16-bit accumulators, two 16-bit index registers, and a 16-bit PC and SP. The addressing range is 24 bits, created by extending a 16-bit address with an 8-bit data- or program-bank register. Microcontroller variations range from a bare-bones ROMless chip with 256 bytes of RAM to controllers with 32 kbytes ROM and 2 kbytes RAM. Specialized peripherals include a 4-channel DMA controller, a DRAM controller, synchronous/asynchronous serial channels, and 4-phase pulse motor drive outputs.

□ **VENDORS/PRICING** Mitsubishi is the developer and sole source of the 37700.

M37702S4LGP (8 MHz, no ROM), $10; M37730M4E (25 MHz, 32 kbytes ROM), $9; M37732S4A (16 MHz, no ROM), $9.50; M37703M2 (8 MHz, 16 kbytes ROM), $8.40; M37702S4A (16 MHz, no ROM), $9.

ARCHITECTURE



The 37700 is a 16-bit, extended 6502. The architecture is accumulator oriented, and a few registers feed directly into the ALU. Instead of the 6502's 8-bit registers, the 37700's registers are 16 bits. And instead of a single accumulator served by 2 index registers, the 37700 has 2 accumulators, 2 index registers, and a 16-bit PC and SP.

The ALU has two bus rails that feed directly into it. Between the rails lie the accumulators, index registers, PC, SP, program- and data-bank registers, and a 24-bit address incrementer. Almost all operations pass through the accumulator. The main registers can function as 16- or 8-bit registers.

In a carryover from the 6502 architecture, the 37700 has a 256-byte "direct page." This page can lie in the first 64-kbyte memory bank or between the first and second banks. The 16-bit direct-page register points to the base, or lower, address of the direct page. Access to the direct page is faster using the direct-page register: It takes only 2 bytes or one instruction word.

The 37700 is pipelined. The CPU fetches the next instruction while executing the current one. A 3-byte prefetch queue holds the next instruction.

The 16-Mbyte address space is divided into 256 64-kbyte banks. The high-order bits of a 24-bit address reference the bank; this field is supplied by an 8-bit program- or data-bank register. Bank 0 holds the special-function registers, internal RAM, and internal ROM spaces. In single-chip mode—executing from on-chip ROM and RAM—the CPU has only one 64-kbyte bank, bank 0. For debugging, the chip can run in microprocessor mode in which it executes exclusively from changeable, off-chip program memory.

The external-memory bus can be multiplexed or nonmultiplexed. For a 16-bit address, the bus is not multiplexed; it uses 16-bit addresses and 8-bit data. The CPU can access 16-bit data from odd or even bytes, but performance will degrade when using an odd byte. Having data aligned on even byte addresses results in the best performance.

Stack—16-bit SP must be initialized on start-up. Typically, SP points to highest addr of internal RAM because a push decrements SP. The SP can be set to an ext memory addr, but stack accesses will be slower.

Addressing modes—28 modes: implied; immediate; accumulator; direct; direct bit; direct indexed X/Y; direct indirect; direct indexed X indirect; direct indirect long; direct indirect long indexed Y; absolute; absolute indexed X/Y; absolute long; absolute long indexed X; absolute indirect; absolute indirect long; absolute indexed X indirect; stack relative; direct bit relative; SP relative; SP relative indirect indexed Y; block transfer.

Special instructions—Increment; decrement; bit set/clear; compare reg to memory; set/clear PSW bits; exchange regs A, B; push/pull regs on/off stack; force break (saves PC, PSW, branches).

Mode	Current (max)	Voltage (V)	Clock (MHz)
Normal	8 mA	3	8
Normal	38 mA	5	25
Stop	20 μA	5	0

In 80-pin QFP.

□ **VARIATIONS**

M37702M2LXXXGP—8 MHz; 16 kbytes ROM; 512 bytes RAM; 8 timers; watchdog; 8-channel, 8-bit ADC; 2 serial I/Os; 68 I/Os; 2.7V parts; 80-pin QFP.

M37702S4LGP—8 MHz, no ROM, 2 kbytes RAM, watchdog, 37 I/Os, 2 serial I/Os, 2.7V parts, 80-pin QFP.

M3773052—8/16/25 MHz, no ROM, 1 kbyte RAM, 8 timers, watchdog, 2-channel PWM port, serial I/O, 64-pin QFP.

M37732S4—8/16/25 MHz; no ROM; 2 kbytes RAM; 8-channel, 8-bit ADC; watchdog; 2-channel PWM port; 37 I/Os; 80-pin QFP.

M37703M2—8/16/25 MHz; 16 kbytes ROM; 512 bytes RAM; 8 timers; watchdog; 8-channel, 8-bit ADC; 2 serial I/Os; 4 PWM timers; 22 I/Os; 64-pin DIP.

M37705S1—8/16 MHz; 512 bytes RAM; watchdog; DRAM controller; 4 DMA channels; 8-channel, 8-bit ADC; 53 I/Os; 100-pin QFP.

SUPPORT

□ **HARDWARE** Emulation pods and evaluation boards available from Mitsubishi.

□ **SOFTWARE** Software tool kit—assembler, C compiler, linker/loader, debugger—from Microtek Research (Santa Clara, CA).

16-bit μP

□ **OVERVIEW** Introduced in 1979, the 68000 set new standards for 16-bit μPs and was the base for the original Apple Macintosh. Its straightforward register-based architecture, orthogonal instruction set, flexible addressing, and advanced memory interface molded a generation of hardware designers. The 68000 is actually a 16- and 32-bit mix—it has 32-bit registers for easy addressing but a 16-bit data path and ALU to conserve silicon. Motorola uses the core in gate arrays as well as the 68302, a communications μC that includes a RISC CPU to process serial line data. Low-power CMOS versions of the μP are available as well as application-specific chips. Toshiba and Philips/Signetics also offer μCs based on the 68000 CPU. The 68000 served as a base for the 680x0 line of 32-bit μPs, which culminated in the 68040.

□ **VENDORS/PRICING** Motorola developed and sells the 68000. Second-source licensees include Hitachi, SGS-Thompson, and Philips/Signetics.

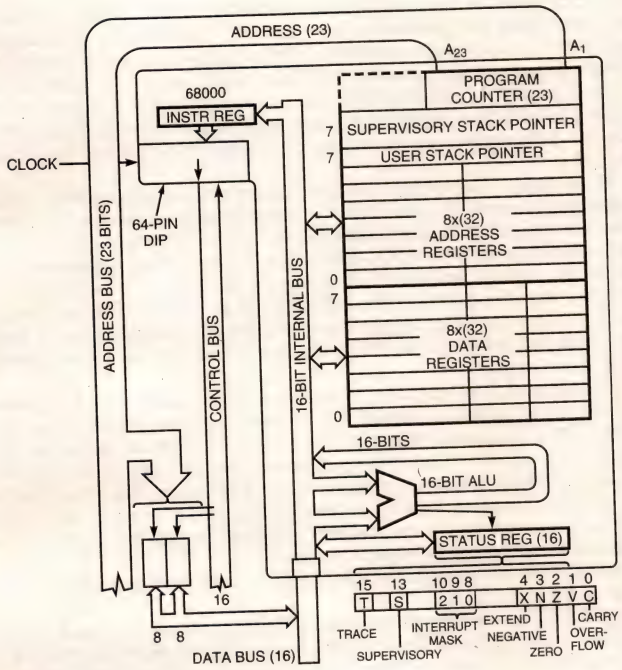
Motorola: 8-MHz 68000, $3.60; 16.7-MHz MC68HC000FN16, $8.65; 20-MHz MC68302, $35.16 (1000); 20-MHz MC68306, $8.95.

Toshiba 68301, $24.55 (100); Philips/Signetics 68070, $17.50 (1000).

Motorola 68000

- 16/32-bit μP: 32-bit regs, 16-bit ALU, 16-bit ext memory
- 18 32-bit user regs, 2 supervisor regs
- 70 instr
- 16-Mbyte addr space
- Nonmultiplexed bus: 24-bit addr, 16-bit data
- Simple asynchronous memory-bus interface
- 68302 communications μC has 68000 core, 1152 bytes RAM
- 68306 has 68000 core, DRAM controller
- 8/10/12/16-MHz clock
- 4-clock reg-reg ADD; 6-clock reg-reg ADD (long); 8-clock reg-reg MOVE
- 12+4n clocks for multiple moves (n words)
- 4-clock NOP (min instr)
- 70-clock MPY; 140-clock DIV
- 4-clock ext-memory R/W
- 378-μsec intr latency

ARCHITECTURE



Engineers have had a love affair with the 68000 architecture for more than a decade. The register-rich processor bridged the gap between 8- and 16-bit as well as 16- and 32-bit processing. Nominally a 16-bit processor, the 68000 has a 16-bit external data bus, 16-bit ALU and data path, and 16-bit orthogonal instructions (most addressing modes apply to all instructions equally). Yet, the CPU has the advantage of 32-bit registers, which opens up addressing beyond 2^{16} bytes. The nonmultiplexed external bus drives 24 address lines and addresses up to 16 Mbytes of memory.

The processor's user and supervisor modes are both implemented in hardware, which eases having a control kernel or OS manage multiple application tasks. The supervisor mode handles interrupt servicing and system functions; the user mode handles application processing. The chip restricts privileged instructions to supervisor mode. These instructions include RESET, STOP, and moves and operations on the status register.

A classic CISC machine, the 68000 has two microcode levels: microcode and second-level, expanded nanocode. Instruction execution triggers a chain of 10-bit microcode words. Each microcode word can reference another word for, say, a jump in microcode or a string of 70-bit nanocode words that directly drive the CPU logic. The original 68000 had enough ROM for 1024 microinstructions and 512 nanoinstuctions.

For its time, the 68000 is register rich. Programmers get eight 32-bit data registers that the CPU can address by bit, BCD, byte, word, or double word. The 7 address registers include user and supervisor stack pointers. Other registers include the 32-bit PC and 16-bit status registers. The SR maintains status for the user and supervisor modes via a user byte and a supervisor byte.

Incorporating memory chips in a 68000-based system has become almost a housekeeping task. The CPU has no memory controller, but the separate data and instruction buses eliminate the need for buffering addresses. However, the CPU needs logic to generate the required DTAK* signal, which marks the successful completion of a memory cycle. An address decoder is necessary for multiple memory chips, and drive buffers may be needed to buffer bus address and data lines. If DTAK* is late, wait states are generated. The 68000 (except EC versions) has an 8-bit, synchronous 6800 bus for peripheral chips.

Stack—Hardware implements 2 stacks—user and supervisor—and pushes and pops PC and SR onto stack for exceptions. Link instr lets you build link lists on private stacks.

Data formats—Byte-oriented addressing: bit, BCD (4-bit), byte, word, and double-word data formats. The 32-bit regs make 24-bit addressing easy. Internal addr regs are 32 bits; the bus is 24 bits. The 24-bit addr are sign-extended to 32 bits.

Special instructions—Can move data between regs, special regs, and memory. Can move up to 16 regs to or from an effective addr, including blocks of data regs to or from addr regs.

□ **VARIATIONS**

68008/68010—68008 has an 8-bit bus for minimal memory configurations; the 68010 implements on-chip virtual-to-physical MMU.

68070—μC with 10/12.5/15-MHz clock, 16-bit timer, UART, I²C serial I/O. 84-pin PLCC or 120-pin QFP.

68302—Protocol-control engine. Includes a supplementary RISC CPU to process line data. 16.77/20-MHz clock, 3 serial communications channels coupled with 6 DMA channels, 3 timers including watchdog, low-power modes, wait-state generator, memory chip select, 1152-byte dual-ported RAM, 28 I/O pins, 132-pin QFP/PGA.

68301—12/16-MHz clock, 8-segment MMU, 3 UARTs, 3 ext intr, 16-bit timer, 16 I/O pins, 100-pin QFP.

68HC000, 68EC000—Low-power CMOS versions. 68EC000 has statically selectable 8- or 16-bit external bus but no peripheral controls.

Motorola peripheral chips—MC6821 peripheral-interface adapter, MC6840 programmable timer module, MC6845 CRT controller, M6850 asynchronous-communications interface adapter, MC6854 data-link controller.

μP	Current (max)	Voltage (V)	Clock (MHz)
68000	280 mA	5	20
68HC000	25 mA	5	25
68HC000	50 mA	5	16.67

In 64-pin DIP; 68-pin QFP, PGA.

SUPPORT

□ **HARDWARE** The 68000 has hardware-development tools ranging from evaluation boards to low- and midrange ICEs and logic analyzers. The best book describing 68000 hardware is Motorola's *The 68000 Family*, Vol 1, (by Werner Hilf and Anton Nausch, Prentice-Hall, Englewood Cliffs, NJ, 1989).

□ **SOFTWARE** Integrated cross-development environments, assemblers, compilers, debuggers, and simulators are all available. Operating software ranging from small real-time kernels to sophisticated operating systems run on the 68000; many of these packages have networked development tools.

□ **OVERVIEW** Sampling in 1991, Motorola's 16-bit 68HC16 μC is a superset of the popular 8-bit 68HC11. The controller is built around three accumulators (one 16-bit, two 8-bit) and three 16-bit index registers. The 68HC16 handles up to 1 Mbyte of memory space by extending the index, PC, and SP registers to 20 bits and operating in one of sixteen 64-kbyte pages. Program and data can share a single address space or have separate spaces. Built for integration on an internal Intermodule bus, the 68HC16 has advanced peripherals including a DSP-like MAC unit. There are five family members, some with up to 48 kbytes of on-chip ROM or flash EEPROM.

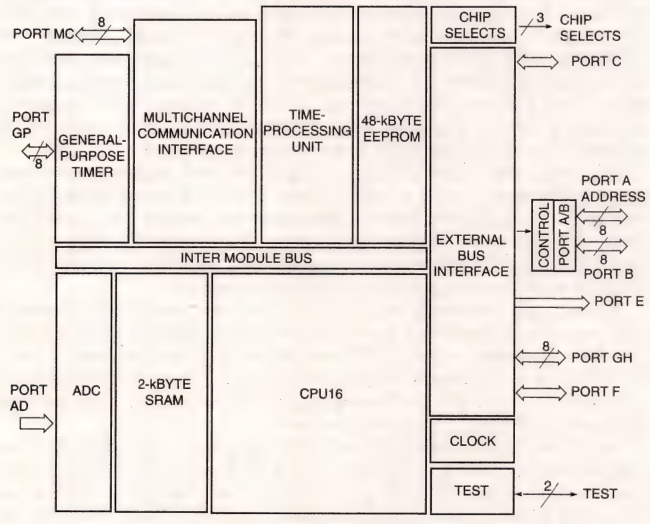
□ **VENDORS/PRICING** Motorola is the developer and sole source of the 68HC16.

68HC16Z1 (1-kbyte RAM, queued serial module, system integration module, 56 I/Os, 132-pin QFP), $14.34; 68HC16Y1 (48 kbytes ROM, 2 kbytes RAM, 99 I/Os, 160-pin QFP), $24.86; 68HC916X1 (48 kbytes flash EEPROM, 2 kbytes block-erasable flash EEPROM, 2 kbytes SRAM, 66 I/Os, 120-pin QFP), $75 (sampling 1Q93); 68HC916Y1 (48 kbytes flash EEPROM, 4 kbytes RAM, multichannel communications interface, 100 I/Os, 120-pin QFP), $75 (sampling 1Q93).

Motorola 68HC16

- Accumulator-based CPU with 2 accumulators, 3 index regs
- Up to 48 kbytes ROM/flash EEPROM (up to 2 kbytes block-erasable)
- Up to 2 kbytes RAM
- 1-Mbyte addr space
- Ext bus: 20-bit addr, 8/16-bit (dynamic) data
- 16-bit MAC unit
- Hardware debug unit
- Watchdog timer
- 7 ext intr
- Up to 99 I/O pins
- PLL boosts 32-kHz or 4-MHz ext clock to 16.78-MHz internal clock; static
- 2 clocks per bus cycle; up to 13 memory wait states
- 120-nsec reg-to-reg ADD, NOP
- 240-nsec mem-to-accum ADD
- 600-nsec MPY; 1440-nsec DIV
- 720-nsec MAC
- 360-nsec LOAD mem-accum
- 3.0-μsec intr latency
- Time-processing unit: 2 counters, 16 channels

ARCHITECTURE



The 16-bit 68HC16 is a superset of the 8-bit 68HC11. All 68HC11 resources and instructions are provided in the 16-bit μC. The 68HC16 goes beyond the 68HC11 by routinely supporting 1-Mbyte addressing and incorporating advanced peripherals, including a DSP-like multiply-accumulate unit (MAC).

Like the 68HC11, the 68HC16 is an accumulator-based architecture. Processing centers around two 8-bit accumulators and a 16-bit E accumulator. The two 8-bit registers can be treated as a single 16-bit accumulator, the D register.

Three 16-bit index registers work in concert with the accumulators. These index registers have 4-bit extensions for creating 20-bit addresses. The extensions are labeled YK for the Y index register, XK for the X index register, and so on. Similarly, the SP and PC—both 16-bit registers—have 4-bit extensions, SK and PK, also giving them 20-bit address capability.

Unlike the 8-bit controller, the 68HC16 has a modular structure built on the Inter Module on-chip support bus—the same bus Motorola uses as base for the 683xx family of specialized microcontrollers. The bus makes adding peripherals easy.

Program and data can share a common address space or use 2 separate spaces. Each space is divided into sixteen 64-kbyte banks. Thus, the 68HC11's 64-kbyte addressing still holds, and old code will run on the 16-bit chip. The 68HC16's addressing space expands to 1 Mbyte, or 2 Mbytes for separate data and code spaces, for larger applications. This scheme delivers a 20-bit extended address to physically address memory. Instruction boundaries are on even boundaries and use little-endian addressing. The CPU accesses words on word or byte boundaries.

68HC11 code compatibility—68HC11 code may need minor modifications to run on 68HC1.

Addressing modes—Immediate (8/16-bit constant), extended (16-bit constant), indexed (8- and 16-bit offsets), indexed (index reg+E accumulator). No base+index addressing. Instead, index regs serve as base to which a constant or another reg can be added.

DSP processing—MAC unit adds two 16-bit regs, 32-bit accumulator. Runs using CPU regs and IX and IY index regs for inputs. Increments indexes automatically for next inputs. One MAC instr automatically decrements loop counter. 720-nsec MAC cycle does MPY+accumulate indexing.

Special instructions—Decrement and increment instr for accumulators and memory words; swap accumulators; exchange regs; transfer SP+1 to index reg; compare memory and 16-bit reg; set SP from index reg; test, set bits using word mask.

68HC16Y1

Mode	Current (max)	Voltage (V)	Clock (MHz)
Run	121 mA	5	16.78
Stop	165 μA	5	0

In 64-pin DIP, 68-pin PLCC.

□ **PERIPHERALS**

General-purpose timer—Includes a compare/capture unit with 1-channel, 16-bit timer; 8-bit pulse accumulator; 9-stage clock prescalar; PWM unit (16-bit free-running counter with 2 channels). Stop mode halts operations.

Queued serial module—2 full-duplex serial communications interfaces: queued serial peripheral interface (synchronous line) and serial communications interface. An intelligent processor, module queues up to 16 commands, which can be repeated; can poll devices and do their processing.

System-integration module—Ext-memory interface has 20 addr, 16 data, and up to 12 programmable-chip-select lines. Includes watchdog, periodic timers; clock generation PLL boosts 32-kHz or 4-MHz ext clock to 16.78-MHz internal clock.

Multichannel communications interface—2 asynchronous, serial-communications-controller lines; 1 synchronous, 3-wire serial peripheral interface.

ADC—8-channel, 8/10-bit ADC with 8 conversion modes, 8 result regs, programmable sample period.

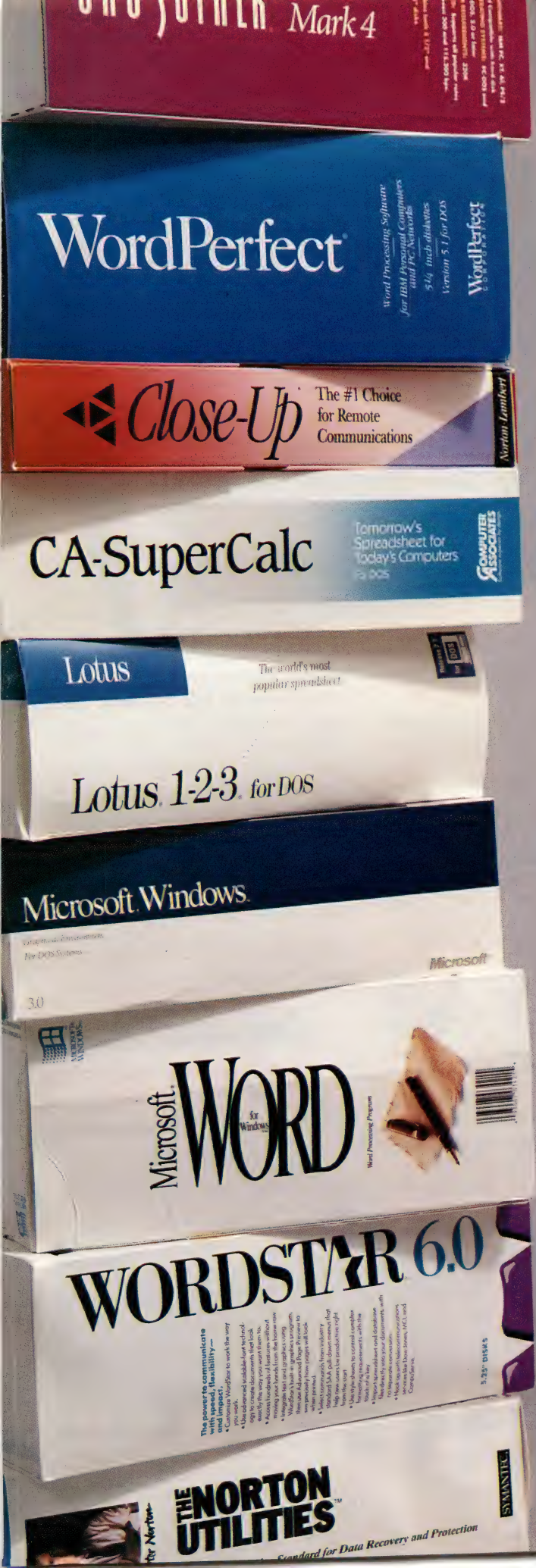
Background mode—For debugging, testing. Stops processor for single stepping, breakpointing. User control via 3 lines. Can read and set regs, memory values from host.

Time processing unit—Handles 16 timer channels; has its own microengine with ROM control store, dual-ported SRAM interface holds parameters. Independent channels have own I/O pin, 16-bit compare-and-capture regs, comparator. Time kept by two free-running counter regs shared by channels. 500-nsec time resolution. Unit has 2 kbytes SRAM.

SUPPORT

□ **HARDWARE** The 68HC16 incorporates a background test mode that aids application debugging. Taking after DSP hardware-assisted on-chip debuggers, the 68HC16's background mode enables external devices to take control of the μC for debugging via 8 control pins. Motorola's ICD16, a low-cost debugging tool, uses the background mode to control a 68HC16 target from a PC. Evaluation boards are available from Motorola. Several ICE and logic-analyzer vendors are porting their hardware tools to the 68HC16.

□ **SOFTWARE** Assemblers, linker/loaders, and C and Modula-2 compilers are available now. A freeware simulator is available, and other simulators are under development, as is a Forth development/runtime system. Two real-time OS kernels are available, and more are coming. Additionally, a DSP filter-design and analysis system (Momentum Data Systems, Irvine, CA) and the GOFAST FPAC.DPAC floating-point libraries (US Software, Portland, OR) support the 68HC16's MAC unit.



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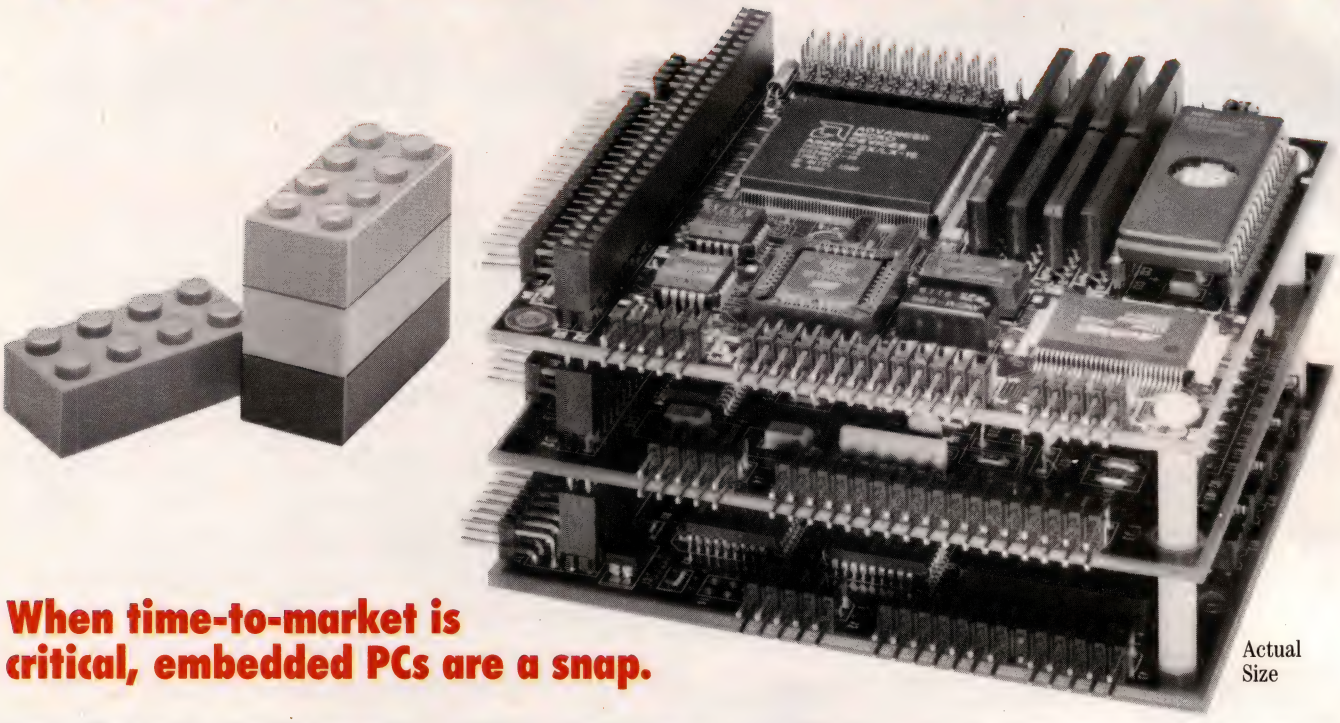
CIRCLE NO. 45

GOOD IDEA. SAME IDEA.



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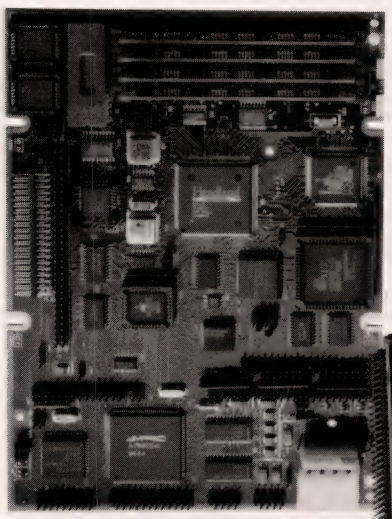
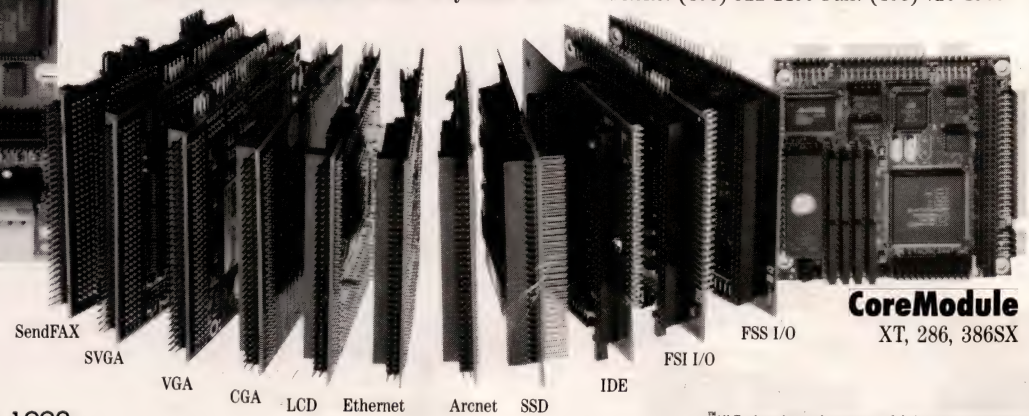


Little Board
PC, 286, 386SX, 386 and 486



CoreModule
XT, 286, 386SX

CIRCLE NO. 38

National Semiconductor HPC

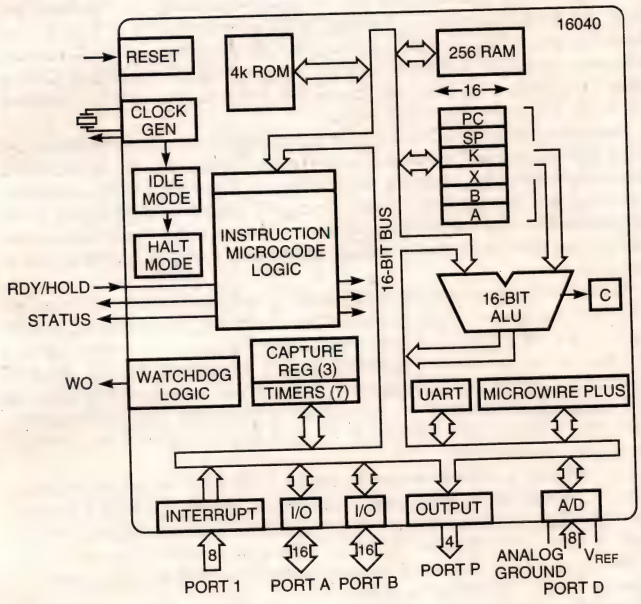
- Accumulator based, 7 regs (8 with MAC unit)
- 62 instr (MAC unit adds 4)
- Up to 1 kbyte RAM
- Up to 16 kbytes ROM
- 64-kbyte addr space
- 16-bit multiplexed addr/data ext bus
- 16-bit MAC unit
- Microwire/Plus serial interface
- 8 16-bit timers, 16-bit watchdog timer
- 4 ext intr
- 31 to 52 I/O pins
- 20/30/40-MHz ext clock (divide-by-2 internal)
- 100-nsec instr cycle at 40 MHz
- 100-nsec reg-reg ADD, NOP
- 3-μsec MPY, DIV
- 400-nsec MAC cycle (MPY, ADD, indexing)
- 2-clock ext mem R/W
- 3 to 5.5V parts
- 7.0-μsec intr latency (for MPY, DIV)

☐ **OVERVIEW** National Semiconductor's HPC family chips are first-generation, 16-bit microcontrollers. Built around a spare set of registers, the microcontrollers deliver high throughput—100-nsec basic instruction cycles—using clock rates as fast as 40 MHz and an effective instruction set. ROM and ROM-less versions are available with a range of peripherals, including a high-speed DSP-like MAC unit, ADCs, PWMs, serial ports, and timers. One chip, the HPC46100, targets servo control by supplementing the core μC with a signal-processing subsystem. The subsystem includes a MAC unit, 8-bit ADC, and PWM signal drivers. Another chip, the HPC46400E, tackles communications with its 4 DMA channels and 2 HDLC (High-level Data Link Control protocol) serial channels. HPC family members come in 68- and 80-pin PLCCs, QFPs, and PGA packages. Programmable idle and stop operating modes help limit power dissipation.

☐ **VENDORS/PRICING** National Semiconductor is the sole source of HPC microcontrollers.

HPC46100 (ROMless, 1 kbyte RAM, MAC unit), $11.40; HPC46003 (ROMless, 256 bytes RAM), $6.10; HPC46064 (16 kbytes ROM, 512 bytes RAM), $7.64; HPC46400E (ROMless, 512 bytes RAM, 4-channel DMA), $9.

ARCHITECTURE



A pioneering 16-bit μC, National Semiconductor's HPC is not a performance slouch. It delivers 100-nsec register-to-register ADDs running with a 40-MHz external clock. Built around a core of 7 registers, the HPC is more than a traditional, accumulator-based μC. It has an accumulator, but operations can take data from memory, operate on it, and return the result to another memory location. Additionally, the CPU can address memory-mapped registers as specific registers or as memory locations.

The HPC's core processor is simple and straightforward: The 7 registers are accessible to the bus and feed directly into the ALU. The chip has a 64-kbyte unified address space for data and instructions. The first 2 kbytes hold the registers and memory-mapped peripheral and control registers. Memory addressing follows a little-endian byte order, and words must be aligned on even byte boundaries.

The 7 registers are the A (accumulator), bytes and X (both indexes), K (loop limit and index), SP, PC, and PSW. The K register is used in conjunction with the bytes register (B) for looping. Many operations automatically increment B by 2 and compare that value to K, which holds the loop limit. When B>K, the loop is completed and a flag set.

HPC chips run with both on- and off-chip memory. External-bus characteristics are programmable. You can program 8- or 16-bit data paths, a multiplexed bus with up to 4 wait states (1 wait state=50 nsec at 40 MHz), and extended memory accessing for slower EPROM or ROM. The μC handles 8- and 16-bit arithmetic. To save memory, the CPU can store and process 8-bit values as bytes. Additionally, 8-bit values are automatically adjusted by the CPU when used in 16-bit arithmetic.

National Semiconductor added a DSP-like MAC (multiply-and-accumulate) unit to help the CPU achieve high-throughput processing. The MAC unit walks through parameter and coefficient tables, accesses table values (B, X, indexes), multiplies the values, and sums the result in a 32-bit register. The unit treats parameter samples as a circular buffer, defined by the A and K registers. The MAC unit runs separately from the HPC core but uses core registers. Hardware defers interrupt processing until any individual MAC cycle completes.

Test and skip—Test and branch is built-in as a test-and-skip instr—do test; if true, skip next instr. Operations test bits, carry/carry* or EQ/NEQ flags, and if source1 is greater than source2.

MAC instructions—MACZ (first MAC iteration; clears MAC accumulator reg), MPY and accumulate, 16-bit MPY, arithmetic right shift.

Special instructions—Decrement/increment; decrement-and-skip (skip next instr if result=0); jump indirect (multiway jump via offset into table of indirect addr); load (with autoincrement/decrement and conditional-skip options); exchange destination with auto increment/decrement and skip options, subroutine return and skip (skips first instr word, used for error returns).

☐ **VARIATIONS**

HPC46003—No ROM, 256 bytes RAM, 8 timer/counters, 32 I/O pins.

HPC46083—8 kbytes ROM, 256 bytes RAM, 8 timer/counters, 52 I/O pins.

HPC46400E—Targets communications. No ROM, 256 bytes RAM, 4 timer/counters, 2 HDLC channels, 4 DMA channels, 36 I/O pins.

HPC46164—No ROM, 256 bytes RAM, 8 timer/counters with 4 input-capture regs, watchdog timer, 8-bit ADC, 52 I/O pins.

HPC46100—Targets servo-control applications. 16 kbytes ROM, 1 kbyte RAM, UART, 31 I/O pins, memory chip select, bus interface. Independent subset—8-bit ADC, 16-bit MAC unit, PWM, timers—interfaces to mechanical subsystem.

HPC46083

Mode	Current (max)	Voltage (V)	Clock (MHz)
Normal	65 mA	5	20
Idle	5 mA	5	20
Halt	200 μA	5	0

In 80-pin PLCC, QFP.

SUPPORT

☐ **HARDWARE** National Semiconductor supplies an ICE and evaluation boards for the HPC family. The ICE has a personality module for different μCs and a built-in PROM programmer. HPC Designer Kits include an evaluation board, C compiler, cross assembler/liner, debug software with a ROM monitor, and hooks for a logic-analyzer interface.

☐ **SOFTWARE** Software tools for the HPC family include National Semiconductor's C cross-compiler, cross-assembler, cross-linker, and librarian. The software runs on PCs and DEC and Sun workstation/servers. The C compiler lets you expand and substitute a function's code for its call to minimize function-call overhead. The HPC46400 has an ISDN basic-rate-interface software package, which implements the CCITT standards for ISDN.

□ **OVERVIEW** Oki's Next Generation 65/66/67K μCs are redesigns of the 8051 family, which Oki second sources. Oki designers sped up execution by devising a new core, adding peripherals, and creating a 16-bit version (67K). Running at 10 MHz, the 65 and 66K deliver a 400-nsec instruction cycle, compared with 1 μsec for a standard 12-MHz 8051. The 65K combines an 8-bit core with an 8-bit external bus; the 66K extends the 8-bit core to 16 bits. The 67K has a new fast 16-bit core, a 200-nsec instruction cycle, and a 16-bit external bus. These μCs are not code compatible with the 8051, but a translator package (and some hand work) can move code from one to another. The static cores let clock rates fall to dc to cut power. Some chips run at 2.7V to further reduce power. Peripherals include a multiply/divide unit, 16-bit timer with capture and compare registers, watchdog timer, and 14-bit time-base counter. Oki supplies OTP versions for fast production and prototyping.

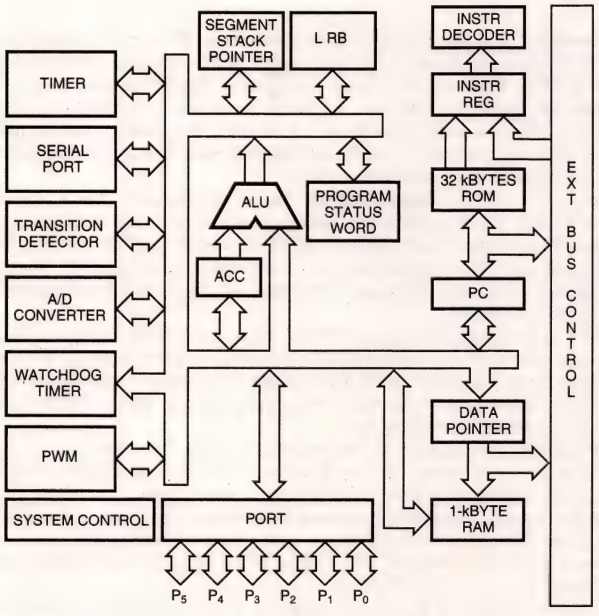
□ **VENDORS/PRICING** Oki developed the 65/66/67K and is the sole source.

MS65512, $3.80 (3V, $4.56); MS65524, $5.15 (OTP memory and ADC, $11.10).

Oki 65/66/67K

- 65K has 8-bit ALU
- 66K has 16-bit ALU, 8-bit ext bus
- 67K has 16-bit ALU, faster bus
- 83 instr
- 4 to 32 kbytes ROM
- 128 to 1024 bytes RAM
- 2 64-kbyte addr spaces
- MPY/DIV unit with 6 regs
- 3 ext intr
- Up to 56 I/O pins
- 10-MHz ext/internal clock, static core
- Cycle=4 clocks (65/66K), 2 clocks (67K)
- Instr take 4 to 9 cycles
- 1-cycle reg-reg ADD, NOP
- 2-cycle mem-reg ADD, LOAD
- 4-cycle MPY; 8-cycle DIV
- 1 cycle per ext memory R/W
- Programmable wait states
- 2.7V (to 4 MHz) versions
- 6.7-μsec intr latency (67K)

ARCHITECTURE



Oki's Next Generation 65/66/67K series μCs build on redesigned 8051 cores, thus taking advantage of current design technologies. The three new cores are the 65K 8-bit core; the 66K 16-bit extension of the 65K core; and the 67K core, which is a full 16 bits. The first two cores deliver 4-clock, or 400-nsec, cycles at 10 MHz. In contrast, a standard 8051 running at 12 MHz takes 12 clocks, or 1 μsec, per cycle. The 16-bit 67K core takes only two clocks, or 200 nsec, for a basic cycle.

The series keeps the 8051's Harvard architecture by having separate 64-kbyte address spaces for instructions and data. The spaces can be combined into a single space by jumpering an external pin. External-memory cycles take 4 clock cycles. Like the 8051, memory-mapped special function registers control peripherals. Data memory is regular; unlike the 8051, there are no specialized segments that require special addressing or logically overlap other segments.

The 8-bit 65K takes after the 8051; both have 4 local register sets mapped in local data memory. One set acts as the current set for processing; switching to a new set makes for a fast context switch because no registers have to be saved in on-chip RAM or external memory. Unlike in the 8051, the 65K has banks of 16, not 8, 8-bit registers. Two of these registers can function as 16-bit registers for addressing, thus replacing the single 16-bit DPTR pointer in the 8051. The A (accumulator), B, SP, and PSW (program-status-word) 8-bit registers are separate.

The 66K took a different tack with registers. The CPU has an accumulator, PSW, PC, local-register base, and system stack pointer. The 66K's registers are organized as sets of 4 local 16-bit registers. Pointing registers are in 8 banks of four 16-bit registers—2 index, 1 data pointer, and 1 user stack pointer. The 16-bit 67K returned to 4 banks of general-purpose 16-bit registers and separate SP, PC, and PSW registers.

Paged memory—8-bit 65K local memory is paged, blocked into 256-byte pages referenced by PSW field. Code can address paged memory using 8-bit reg. Main-memory accesses require 16-bit addr. 65K makes a distinction (as does 8051) between local, 8-bit addressable paged memory and general, 16-bit addressable memory. 65K addr modes differ from 16-bit 66/67K modes.

Bit manipulation—Set, reset, complement bit. Can complement carry bit or transfer a bit to or from carry. Bit operations not restricted (as in the 8051)—can be anywhere in memory. Also bit set/reset in PSW.

Special instructions—Exchange, 1/2 byte swap, increment/decrement memory (8 and 16 bit), compare (8 and 16 bit), decrement reg and jump if 0 or not 0, indirect jump (on regs A, B 65K), stack push and pop, call or return if carry or zero is set (65K), string move/transfer/compare (66/67K), execute data as instr (66/67K), complement (8 and 16-bit), predecrement and postincrement addressing (67K), memory indirect addressing, and indirect reg call (67K).

□ VARIATIONS

MSM65511—4 kbytes ROM, 128 bytes RAM, 2 8-bit timers, watchdog timer, 14-bit time-based timer, 16-bit timer with capture and compare regs, 32 I/O pins, 2.7 or 5V, 40-pin DIP, 44-pin QFP.

MSM65512—8 kbytes ROM, 256 bytes RAM, 3 8-bit timers, watchdog timer, 16-bit timer with capture and compare reg, UART, 32 I/O pins, 2.7 or 5V, 40-pin DIP, 44-pin QFP.

MSM65516—32 kbytes ROM, 640 bytes RAM, 3 8-bit timers, watchdog timer, 16-bit timer with capture and compare reg, UART, 32 I/O pins, 2.7 or 5V, 64-pin DIP/QFP.

MSM66201—16 kbytes ROM; 512 bytes RAM; 4 16-bit timers; 2 PWMs; watchdog timer; 8-channel, 10-bit ADC; UART; 48 I/O pins; stop, halt, hold power modes; 64-pin DIP/QFP.

MSM66207—32 kbytes ROM; 1024 bytes RAM; 4 16-bit timers; 2 PWMs; watchdog timer; 8-channel, 10-bit ADC, serial I/O port; 48 I/O pins; stop, halt, hold power modes; 64-pin DIP/QFP.

MSM67620—16 kbytes ROM, 512 bytes RAM, 3 16-bit timers with 4 capture/compare regs, 2 8-bit timers, serial I/O port, 56 I/O pins, stop and halt power modes, 64-pin DIP/QFP.

Chip	Current (max)	Voltage (V)	Clock (MHz)
66201	35 mA	5	10
67620	38 mA	5	10
65512	30 mA	5	10
65512	15 mA	3	5

In static 64-pin DIP, 68-pin PLCC.

SUPPORT

□ **HARDWARE** Evaluation boards and ICEs are available from Oki.

□ **SOFTWARE** Development tools from Oki include a relocatable assembler/linker.

16-bit μC

□ **OVERVIEW** Introduced in 1989, the Siemens 166/167 targets the high end of 16-bit embedded processing. It combines a 40-MHz RISC-like CPU with a raft of peripherals for complex applications such as automotive, motor, servo, and industrial control. Not inexpensive, the Siemens 80C166/167 is one of the fastest 16-bit μCs with a 100-nsec/instruction peak execution rate. The chip's modular architecture makes adding peripherals easy. Siemens plans to use the 166 as an ASIC core. A joint development with SGS-Thomson produced a chip integrating the 166 μC with 32 kbytes of flash EPROM.

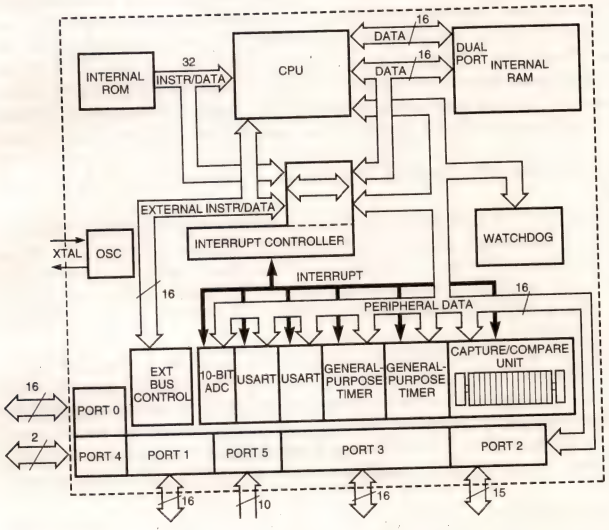
□ **VENDORS/PRICING** Siemens developed and sells the 80C166/167 μC. SGS-Thomson sells the ST10, which is an 80C166 with 32 kbytes of flash memory.

80C166 with no ROM, $22; 83C166 with 32 kbytes ROM, $26. 80C167, $30; the chip is sampling now, and production is slated for 1Q93.

Siemens 80C166/167

- RISC-like μC has 4-stage pipeline, 100 nsec/stage
- Banks of 16-bit regs in RAM (banks are 1 to 16 regs)
- Up to 32 kbytes ROM/flash EPROM
- 1 to 2 kbytes data RAM; 1 kbyte dual ported (R/W)
- One 256-kbyte to 16-Mbyte addr space
- 8/16-bit ext bus, 4 bus modes
- Peripheral-event controller handles 8 I/O events via DMA
- 1 or 2 capture/compare units; each has 16 channels, 2 timers
- 10-bit ADC, 4-channel PWM, 2 serial ports, 38 ext intr
- 40-MHz ext clock (can drop to 2 MHz), 20-MHz internal
- 1-cycle instr execution (pipelined); 100-nsec ADD, NOP
- 500-nsec MPY, 1-μsec DIV (both interruptible)
- 100-nsec ext-mem R/W, programmable wait states
- 10-bit ADC, 9.75-μsec conversion time
- 850-nsec peripheral-event controller, 400-nsec sample rate
- 78-kHz max PWM, 8-bit resolution
- 850-nsec intr latency
- 450-nsec latency for high-speed intr

ARCHITECTURE



The Siemens 166/167 μC has many RISC-like features: a 4-stage pipeline (fetch, decode, execute, write back), 1-cycle barrel shifter, and fast multiply/divide function unit. The 166 also has a reduced instruction set of 76 instructions (79 for the 167). Pipeline stages are clocked in 100-nsec cycles, so most instructions appear to execute in a single cycle. Instruction latency is 4 cycles, or 400 nsec.

Operations center around 16-bit registers in banks of up to 16. These banks are in dual-ported RAM, which lets the CPU read a register for the next operation while writing back the results of the current operation to another register. The SCXT instruction switches context from one bank to another by changing the context pointer, thus minimizing context-switch time.

Instructions are 2 or 4 bytes long. Unlike many 8- and 16-bit μCs, the 166/167 can handle a 4-byte (double-word) instruction fetch from on-chip ROM in one 100-nsec stage. A single fetch gets an entire instruction, thus speeding execution. However, off-chip program accesses suffer at least a 1-cycle stall for 4-byte instructions because the 16-bit external-interface bus permits only a single-word fetch.

The 166/167 caches branch-target instructions and uses them to supply the next iteration of a branch. This caching lets branches execute without stalling the pipeline. First-pass loop branches pay a single-cycle penalty. Nonaligned, double-word, branch-target instructions also pay a 1-cycle penalty. Compare and increment/decrement instructions speed loops.

The CPU addresses up to 256 kbytes (166) or 16 Mbytes (167) of the unified instruction-data memory space. The μCs carry up to 32 kbytes of program ROM or flash EPROM and 2 kbytes of data RAM. The sophisticated external-memory bus has 4 programmable modes and a wait-state generator. The bus can partition physical memory into multiple segments each having a different type of memory.

User and system stacks—User stacks can be anywhere in memory; system stack is in high memory at a fixed location.

Interrupt priority levels—16 priority levels partitioned into 4 groups; eases the programming necessary to separate and process multiple events.

Segments and pages—μC addresses up to 256-kbyte (166) or 16-Mbyte (167) addr space via code segmentation or data paging. Addr space divided into 64-kbyte program segments, 16-kbyte data pages. Code-segment pointer references current code segment; 4 data-page pointers reference data pages. In nonsegmented mode, CPU has one 64-kbyte addr space.

Sequence instructions—167 has instr that ease addressing and control intr. Atomic instr freezes intr and peripheral-event-controller service for up to 4 subsequent instr. Instr is much safer and faster than setting and resetting control-word flags. The extend-segment/page instr lets code (compilers mainly) bypass data paging for up to 4 instr.

PERIPHERALS

Peripheral-event controller—Offloads CPU by servicing up to 8 I/O channels. Uses DMA to bypass CPU, steals bus cycles, increments pointer for up to 255 iterations. Counts down service counter for each channel and interrupts CPU at zero. The 166 has 1 capture/compare unit; the 167 has two. Each unit has 16 capture channels and 2 timer/counters.

PWM—Modulates duty cycle; has 4 channels and 8-bit resolution up to 78 kHz (167).

Timers—Five 16-bit up/down timer/counters; watchdog timer.

ADC—10 to 16 channels, 10-bit resolution, 4 conversion modes.

2 serial channels—With baud-rate generator.

Hold/Acknowledge external bus—Can program so ext devices take control of ext bus for critical data transfers. Processor hangs on bus until an acknowledge.

Segmented physical memory—Can divide space into 5 addr ranges with or without wait states.

External-memory interface—Has programmable chip selects and memory controller with wait-state generator (0 to 15 50-nsec states). Minimizes glue logic.

32 to 52 interrupt sources—Organized into 16 priority levels, partitioned into 4 groups. 167 has 38 ext intr.

Mode	Current (166/167, max)	Voltage (V)	Clock (MHz)
Run	180 mA	5	40
Idle	20/25 mA	5	40
Power down	100 μA	2.5	0

166 in 100-pin QFP; 167 in 144-pin QFP.

SUPPORT

□ **HARDWARE** Instructions that aid debugging include software trap, which shifts control to debug software; software reset; and a service watchdog timer. Siemens and third-party vendors sell evaluation boards. Bondout chips are available from test-equipment vendors.

□ **SOFTWARE** A macroassembler/linker/loader and simulator are available from Siemens. The simulator is compatible with Siemens' ICE. C, Modula-2, and Forth compilers are available from software vendors. A real-time operating system has been ported to the 166/167.

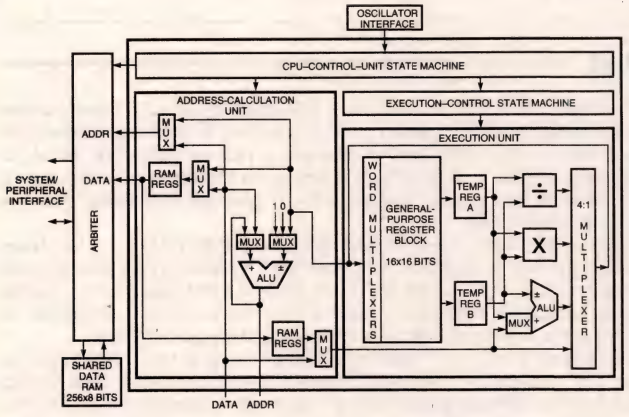
□ **OVERVIEW** Fuzzy logic has emerged as an alternative technology for low- to mid-range control applications. Togai Infralogic's pioneering FC110 is a specialized 16-bit μP that runs fuzzy-logic applications. Designed as a coprocessor, the FC110 handles as many as 220,000 fuzzy-rule evaluations per second for systems with up to 800 fuzzy rules. Fuzzy applications written in Togai's Fuzzy Processing Language are portable: They can run on the FC110, other supported μCs, or standard C hardware platforms. Togai has integrated FC110s onto VMEbus and SBus cards as well as a stand-alone single-board computer. Togai's fuzzy-logic software includes an interactive, graphical development environment for creating fuzzy systems. A second-generation Togai fuzzy processor is available as an ASIC core from VLSI Technology. This processor can evaluate one million fuzzy rules per second.

□ **VENDORS/PRICING** Togai Infralogic developed the FC110 and is the sole supplier. FC110s cost $40 (1000).

Togai FC110

- Fuzzy-logic μP; 16-bit instr, regs
- 19 instr (6 fuzzy logic)
- 16 regs hold data, addr
- 64 bytes dual-ported RAM, shared with host
- 256 bytes data RAM
- 256 bytes memory-mapped I/O
- 128-kbyte ext addr space for program, fuzzy rules
- Ext bus: 16-bit addr, data; multiplexed or nonmultiplexed
- 8-bit peripheral/host interface (6-bit addr)
- 20-MHz ext clock (divide-by-2 internal)
- 100-nsec reg-reg ADD, NOP
- 500-nsec mem-reg ADD
- 200-nsec MPY, 1×3 bytes; 5-μsec DIV
- 100-nsec min ext-mem R/W
- 220,000 fuzzy evaluations/sec
- Holds up to 800 rules
- 266 μsec—evaluates 35 rules, 10 inputs; 3 outputs
- 5.4 msec—evaluates 150 rules, 50 inputs; 10 outputs

ARCHITECTURE



Tailored for fuzzy-logic applications, Togai Infralogic's FC110 is a specialized, 16-bit μP. Of its 19 instructions, 6 are hard-wired fuzzy-rule operations. FC110 addressing is structured for fuzzy processing.

Register-oriented, the FC110 is built around a block of 16 16-bit general-purpose registers. These registers feed into temporary registers that pass register values to one of three functional 16-bit units: the ALU, fast multiplier, or divider. There is a separate ALU address-calculation path. The FC110 has no on-chip program memory, but a 256-byte RAM serves as data memory. External memory holds program code and constants. Data RAM and external memory have different address spaces. Data-memory arithmetic and logical operations are byte, word, 3-byte, or double-word in size. Hardware automatically handles operand adjustments and schedules multiple cycles as needed.

Fuzzy logic is a mathematical offshoot of artificial intelligence and expert systems. A fuzzy-logic system converts inputs into linguistic variables. These variables have a degree of truthfulness that ranges from 0 to 1 for characteristics, or membership functions, such as SLOW. The variables are used in rules, such as IF((SPEED IS SLOW) and (ANGLE IS MEDIUM)), THEN (THROTTLE IS FASTER).

SPEED, ANGLE, and THROTTLE are linguistic variables; SLOW, MEDIUM, and FASTER are membership functions. The FC110 processes rules in parallel: It evaluates rule antecedents, generates results from the consequent portion, then sets result variables. Multiple rules can produce the same consequent variables. The FC110 combines these variables and converts them into defuzzified, scaled output parameters to drive external software and hardware.

FC110s serve as coprocessors to a host CPU. The FC110's host/peripheral interface links an external host to the fuzzy-logic processor via 64 bytes of dual-ported RAM. Two RAM locations serve as input and output control registers. The host processor or an I/O controller interfaces to the external system, gathering input parameters and shipping them to the FC110 for processing. The μP returns the output control parameters.

Addressing modes—Instr can be byte, word, 3-byte, or double-word oriented. Modes include immediate, memory direct, reg direct, memory direct indexed, data memory indirect pre-increment, data memory indirect post-decrement. Data memory accesses have increment/decrement.

Fuzzy-logic instructions—Fuzzy-AND finds minimum between 2 data values and sets flag; Fuzzy-OR finds maximum between 2 data values and sets flag; Right-Hand-Side Compute computes result for rule using centroids, combines results; RSCH computes right-hand-side result by height not centroids; Left-Hand Side Compute computes left-hand side of fuzzy rule; Defuzzification defuzzifies right-hand-side results, by division.

Special instructions—Set operation/function modes for chip interfaces; compare regs, memory, bytes, or words; stop and wait for system message to set status bit. Jump-to-subroutine and return-from-subroutine instr use RAM stack.

□ INTERFACES

Coprocessor interface—The FC110 is slaved to a host processor or I/O controller on an 8-bit interface. Reading or writing to the first two words of the FC110's RAM area (output- and input-communications regs) interfaces to the host. Hardware interprets a write, setting the Int (system-intr) signal active. Set mode programs the host interface to model one of two CPU interfaces: that of the Intel 8051 or Motorola 6800. The interface can be multiplexed; 8-bit data, 6-bit addr, sharing lines or not.

Program/knowledge base—Program code and fuzzy-logic knowledge base are in off-chip 16-bit memory. The FC110 handles up to 64k words (128 kbytes) ext memory. Program/knowledge-base memory has addr space separate from on-chip data memory.

Int signal—System interrupt. Indicates to host that FC110 has written to the peripheral output-communications reg. Once host reads this reg, the pin is inactive (high).

Memory interface—Nonmultiplexed set of 16-bit addr and 16-bit data ext buses. 90-nsec min for addr cycle—effectively, 2 clock periods, or 100 nsec.

Idle signal—Indicates that FC110 is in idle mode (active low) waiting for a signal.

68HC05K1

Mode	Current (max)	Voltage (V)	Clock (MHz)
Run	206 mA	5	4
Wait	0.9 mA	5	4
Stop	1 μA	5	0

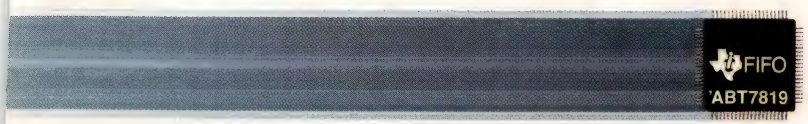
In 16-pin DIP, SOIC.

SUPPORT

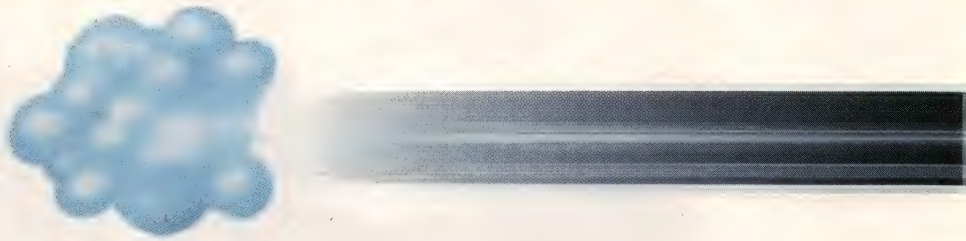
□ **HARDWARE** Zax Corp (Irvine, CA) supplies an ICE for the FC110. Togai has an FC110 Development Module—an FC110 on a 2.5×4-in. single-board computer with 128 kbytes of program/knowledge-base EPROM. Additionally, FC110s are available on a VMEbus board, SBus card, and a single-board computer with digital- and analog-control interfaces. The VMEbus board holds up to four FC110 subsystems; the SBus card holds two, each with 128 kbytes of program/knowledge-base EPROM. Second-generation fuzzy μP is available as an ASIC core.

□ **SOFTWARE** Togai sells a full set of development software for the FC110. The TIL shell is a Windows-based, graphical development environment. TIL utilities include model, timing, chart, and watch editors; watch windows; and a control-surface-plot utility. You program the chip using Togai's Fuzzy Programming Language—a block-structure, object-oriented language. Code can be compiled to the FC110 or to the Fuzzy-C Development System, which generates portable C code that runs on standard platforms. Togai offers development kits for several μCs.

FASTEST IN.



FASTEST OUT.



THE NEW 80-MHz 'ABT7819 FIFO FROM TEXAS INSTRUMENTS.

Introducing the industry's first 80-MHz FIFO, the SN74ABT7819. It's the newest addition to a full line of high-performance, clocked, 18-bit FIFOs from Texas Instruments. And it can run circles around the FIFOs you're using now.

Blazing speed with excellent metastable characteristics

Based on our power-saving Advanced BiCMOS technology, the 'ABT7819 has a maximum access time of 9 ns (measured at C_L = 50 pF). It's the first to offer such performance. And its unique multistage synchronization circuitry greatly improves the metastable characteristics of status flags. That makes it an excellent choice for today's high-speed multiprocessing systems—or any system where speed and reliability are paramount.

BIDIRECTIONAL FIFOs

Device	F max (MHz)	Max access time (ns)	Data setup time (ns)	Data hold time (ns)
'ABT7819	80	9*	3	0
'72615†	40	15	6	1
'5420‡	40	16	12	0

* C_L = 50 pF vs. standard 30 pF test load.
Specs based on manufacturers' data as of April 1992,† July 1992‡

Highly integrated in a choice of standard packages

The bidirectional 'ABT7819 is more than just two 512-word-deep by 18-bit-wide FIFOs sitting side by side. It's bidirectional control logic, flag logic, latches and synch circuitry integrated into a single package to simplify your designs.

The 'ABT7819 comes in compact 80-pin SQFP (actual size 14 mm x 14 mm tip to tip) and standard QFP packages to help save valuable board space. Plus, it's available in −12-, −15-, −20- and −30-ns cycle times for easy performance upgrades.

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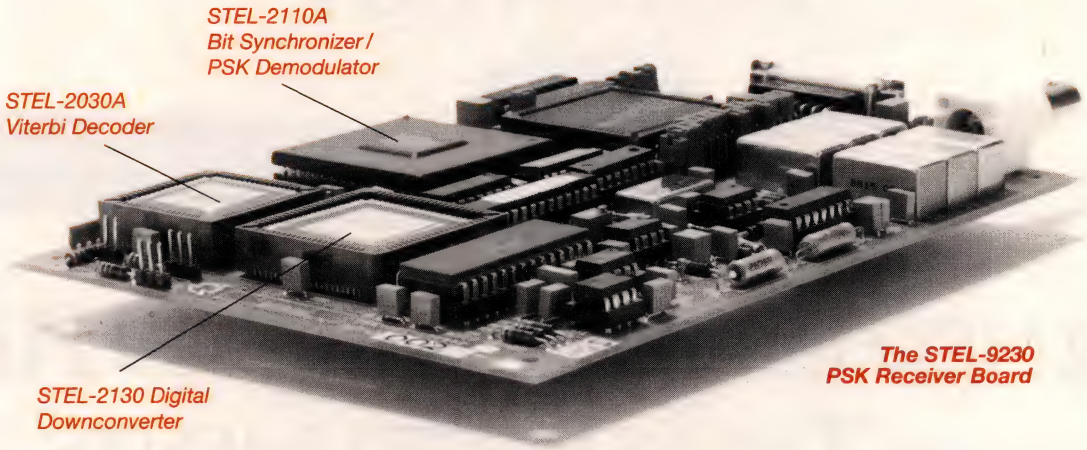
For more information on the SN74ABT7819, use the reader service number below or contact your local TI sales office. We'll have you up to speed in no time.

TEXAS INSTRUMENTS

00-7536B

CIRCLE NO. 47

Digital PSK Demodulation



- *BPSK, Coherent DBPSK & QPSK Demodulation*
- *9.6 Kbps to 256 Kbps (BPSK) and 512 Kbps (QPSK) data rates*
- *70 MHz input carrier frequency, up to ± 1 MHz frequency tracking range*
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Stanford Telecom continues its leadership in reducing complex communication systems to silicon with the STEL-9230 Digital PSK Demodulation Board. Timing recovery, demodulation, downconversion, carrier correction and Viterbi decoding are all performed by Stanford Telecom ASICs, giving you highly stable, robust and predictable performance.

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ADN-101

CIRCLE NO. 48

AMD 29000

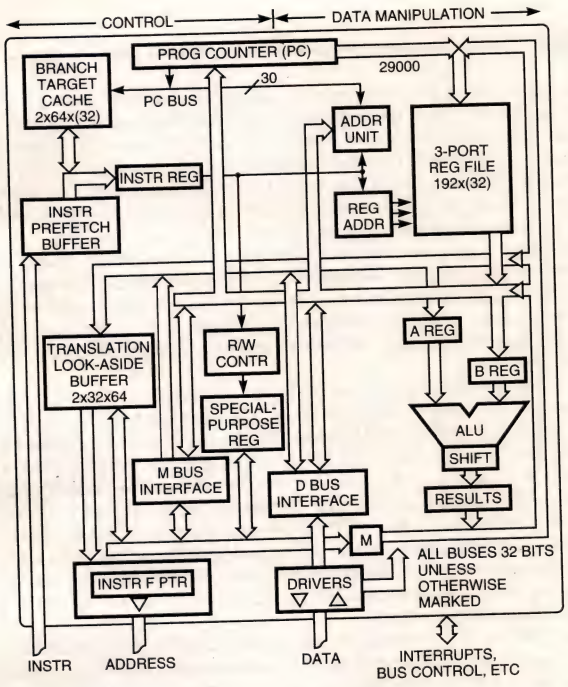
- RISC CPU, FPU coprocessor
- 115 instr (125 for 29050 with FPU)
- 4-stage pipeline
- 192-reg reg file (3 ports with reg windows)
- 512 bytes/1 kbyte branch-target cache (29035/30, 4- or 8-kbyte instr cache)
- On-chip, 64-entry MMU
- No hardware integer MPY, DIV
- 4-Gbyte addr space
- 3 ext 32-bit buses: addr, data, program
- 4-clock intr latency
- 16/20/25/33/40-MHz clock
- 1-clock execution (pipelined)
- 23 native MIPS peak (33 MHz)
- 1.6 cycles/instr, 29000 with branch-target cache; 1.26 cycles/instr, 29030/35 with instr cache
- Reg windows cut context-switch time
- Single-cycle branches with branch target in branch-target cache.
- 1-clock mem R/W
- Burst-mode mem access, 1-kbyte block

□ **OVERVIEW** Originally developed for Unix workstations, Advanced Micro Devices' 29000 emerged too late to compete against the already entrenched SPARC and Mips RISC μPs. AMD then successfully retargeted the processor for embedded systems. Today, the 29000's large applications base includes laser printers, X-terminals, graphics, and networking. The 29000 is an example of one of the two major embedded-systems RISC architectures, and designers like the processor's clean memory interface and simple operation. The μP has a large, 192-register register file and no on-chip cache. Later versions added an FPU, on-chip caches, and embedded-application peripherals.

□ **VENDORS/PRICING** Advanced Micro Devices developed the 29000 family and is the sole source.

29000 (16 MHz, QFP), $59; 29200 (16 MHz, QFP), $51; 29005 (16 MHz, QFP), $48; 29050 (16 MHz, PGA), $198; 29030 (20 MHz, QFP), $74; 29035 (16 MHz, QFP) $54.

ARCHITECTURE



A classic second-generation RISC chip, the 29000 CPU delivers a sustained performance of 1.26 to 1.6 cycles/instr. The 29000's RISC characteristics include a pipelined load/store architecture, reduced instruction set (115 instructions), no hardware integer multiply or divide, and simplified exception processing.

What makes the 29000 unique is its large register file: 192 32-bit registers. Triple ported, the register file handles two operand register reads and one register result write in a single clock. The register file can also do on-chip stack operations and register windowing.

Another unique feature is the branch-target cache. Two-way set-associative, the cache holds up to 128 instructions in 4-word blocks. The first 4 instructions of a branch target are cached in the cache, waiting for the branch to repeat. When the branch does repeat, the cache furnishes the instructions, thus keeping the branch-penalty time to 1 cycle. The branch-target cache is effective for loops, which pay a penalty for only the first branch pass.

The 29000 CPU is built around a simple 4-stage pipeline: fetch, decode, execute, and write-back. Most 29000 instructions specify 3 addresses—two registers as inputs and a register for the result. Eight-bit addresses specify a register in the register file. The addresses are divided into local (MSB=1) and global (MSB=0), and 128 registers are in the local set.

The 29000 memory interface provides single-cycle access for DRAM, page-mode DRAM, or ROM. A Harvard architecture, the 29000 has separate program and data buses as well as a common, pipelined address bus. Unlike many RISC processors, the 29000's external memory can pump instructions in at the CPU clock rate to deliver cache-like performance. A DRAM controller, the Am29C668, runs both standard and page-mode DRAM for the 29000 but requires some external control logic and DRAM buffers. The 29200 incorporates a DRAM and ROM controller and handles both big- and little-endian addressing.

User/supervisor modes—Protected operation in supervisor mode.

Compare—Puts results into general-purpose reg instead of using condition codes in a status reg. Makes processing more general because the reg can hold multiple conditions. Asserts compare conditions and, if not true, cause software trap. Asserts include tests for equality, nonequality.

Move—Moves multiple bytes, half words, or words between regs and memory. Cuts overhead for moving data to/from memory.

Instruction spaces—Two spaces: instr/data memory and instr ROM, for embedded applications with EPROM.

Multiprocessing—LOADSET implements binary semaphore: Loads reg, locks memory (LOCK* asserted), writes back all 1s. Load-and-lock and store-and-lock instr read or write memory location with LOCK* asserted during the memory access.

CLZ instruction—Counts leading 0s in word, can speed bit-map processing by finding first non-zero bit. CPBYTE compares words by byte and sets Boolean result into reg.

□ **VARIATIONS**

29000—Classic 29000 with branch-target cache and MMU, no FPU. 16/20/25/30 MHz, 169-pin PGA.

29005—Stripped-down version without MMU or branch-target cache. 16 MHz, 168-pin QFP.

29030/35—Simplified CPU, data and instr share ext bus, uses 8-kbyte (2-way set-associative) or 4-kbyte (direct-mapped) cache. 1.26 cycles/instr typ. Has 8/16/32-bit ROM interface. 25/33 MHz, 145-pin PGA; 16/20 MHz, 144-pin QFP.

29050—Integrates 29000 with on-chip FPU. Has instr for floating-point operations; FPU handles integer MPY and DIV. 20/30/33 MHz, 169-pin PGA.

29200—CPU integrated with peripherals and logic. Has 7 DMA channels, UART, parallel port (IBM PC), timer, 16 I/O pins, 7 intr, ROM and DRAM controllers, laser-printer "video" interface, and peripheral-interface adapter. 16 MHz, 168-pin QFP.

29205—Stripped-down 29200. Has 16-bit data bus, 2 intr, 3 serial ports, and 2 DMA channels. 16 MHz, 100-pin QFP.

μP	Max current (at 5V)(A)	Pins, package	Clock (MHz)
29000	3.63	169-pin PGA	33
29005	1.76	168-pin QFP	16
29050	4.4	169-pin PGA	40

SUPPORT

□ **HARDWARE** ICEs, logic analyzers, and development boards are available from third-party vendors. Plug-in evaluation boards are available from AMD. PC-form-factor 29000 mother boards are also available for development.

□ **SOFTWARE** C, C++, Ada, Pascal, and Fortran compilers and source-code debuggers are available from major software vendors. Cross-development tools run on PCs as well as most Unix-based workstations including Sun, HP, and DEC. Real-time OS kernels are also available.

□ **OVERVIEW** The Acorn, or ARM, μP was developed initially by Acorn in 1983 for personal computers in Europe. The ARM (Advanced RISC Machine) μP, as it is known now, has been redirected toward low-power, portable, and embedded applications. Apple uses the ARM as the base for its soon-to-emerge "Personal Digital Assistant." Recent ARM processors are built around the ARM6—a small (106×165 mm) static core fitted with 4 kbytes of unified cache and an on-chip MMU. The latest chip, the ARM250, integrates DRAM and video controllers with an ARM CPU core.

□ **VENDORS/PRICING** Advanced RISC Machines (ARM), a joint venture of Acorn, Apple, and VLSI Technology, owns the ARM design and licenses it for production. VLSI Technology sells ARM chips, as well as ARM CPU macrocells for ASICs with CPU clock rates to 30 MHz. GEC Plessey Semiconductor is also licensed to sell the chips.

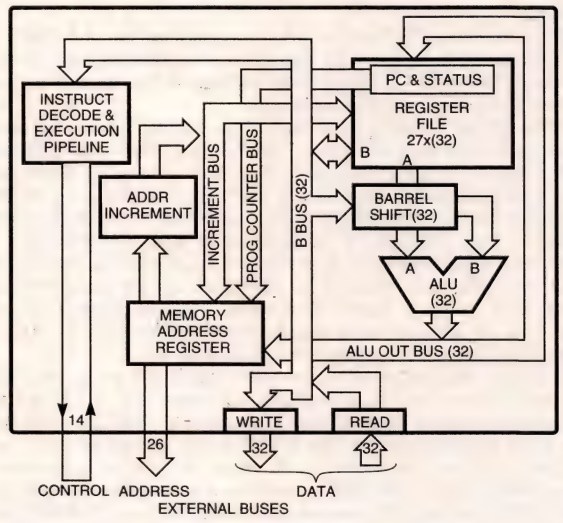
VLSI Technology Inc: VY86C600 (ARM6 core, 4 kbytes cache, MMU, coprocessor interface, 160-pin QFP), $48.81; VY86C610 (ARM6 core, 4 kbytes cache, MMU, 144-pin QFP), $46.49; VY86C060 (ARM6 core, 32-bit addr and data buses, 100-pin QFP), $33; VY86C061 (ARM6 core; 32-bit data, 26-bit addr buses; 84-pin PLCC), $28.85. (All prices for 1000-unit qty).

GEC Plessey: ARM250 (ARM2aS core; 20-bit addr bus; memory, video, and I/O controllers; 160-pin QFP), $25.

ARM VY86Cxxx

- 31 general-purpose regs, 16 in bank
- 44 instr, 10 types
- 365,000 transistors (ARM 600)
- 4-kbyte unified cache, 64-way set associative
- 32-bit addr space
- 32-bit nonmultiplexed ext instr and data buses
- MMU with 32-entry TLB
- Synchronous/asynchronous memory
- No DIV instr
- 2 ext intr (1 fast)
- Coprocessor interface (except 610)
- DC to 20-MHz ext clock (divide-by-1 internal)
- 1.8 clocks/instr
- Instr set compacts code for multiple operations per instr
- 1-cycle reg-reg ADD; 4-cycle reg-mem ADD
- 680-nsec MPY
- 40-nsec NOP at 25 MHz
- 3-cycle mem R/W
- 5 mA/MHz power dissipation
- 1-μsec intr latency

ARCHITECTURE



The original Acorn was a silicon miser, using only 24,000 transistors and dissipating 0.5W. Now implementing modified RISC techniques, the ARM (Acorn RISC machine) has a 2-stage (decode and execute) pipeline and achieves single-cycle instruction execution. But unlike a classic RISC μP, the ARM does not have a load/store architecture—ALU operands can come from memory. The processor has a block-data-transfer instruction to load and store data from any subset of the general-purpose registers.

The ARM has a minimal instruction set of 10 instruction types, yet the instructions are complex. All instructions execute conditionally—their execution depends on an encoded test, which can test conditions such as equal, not equal, clear, negative, overflow, no overflow, and always. The ARM has no shift instruction; instead, all ALU operations have a shift option that precedes them.

Like most early RISC μPs, the ARM has no integer divide instruction. It does, however, have multiply and multiply-and-accumulate (MAC) instructions. The MAC instruction speeds math-intensive applications. A Booth hardware multiplier operates on two operand bits at a time to build a final product. A 32-bit multiply takes 16 cycles; smaller multipliers reduce the number of cycles.

Early ARM μPs ran directly out of memory, which limited performance. Later versions based on the ARM6 core have a 4-kbyte unified on-chip cache. This 64-way set-associative cache holds 64 4-word lines. The CPUs also have an MMU for translating between virtual and physical addresses as well as controlling access permissions. The ARM600 and 610 can do memory-section and page-based accesses.

The ARM has 31 general-purpose registers, but the CPU can address only 16 as part of the local register set. Multiple-operation instructions help compact code but add to execution time. The shift option for ALU instructions takes an extra cycle. Nontaken branches cause a delay of up to 3 cycles. A taken branch incurs no penalty.

The 26-bit ARM2 bus is expanded to 32 bits for the ARM600. The external bus is not multiplexed. The ARM600 bus clock can be synchronous or asynchronous with respect to the cache clock. The ARM600 also has a write buffer, which lets execution continue while writes are pending. The buffer holds 8 data words with 2 addresses.

Modes—User and supervisor. 4 exception-processing modes: intr request, fast intr request, abort mode, and undefined mode. Modes use different reg windows to overlay some of the 16 general-purpose regs.

Coprocessor interface—Enables another CPU to load or store data or request a CPU operation. 610 has no coprocessor interface.

Branches—Branches, like other ARM instructions, are conditional. Branch with link writes old PC into R14 for a return. Branches have 24-bit offset from current PC.

VY86C060

Current (max)	Voltage (V)	Clock (MHz)
37.7 mA	5	25

In 100-pin QFP.

□ **VARIATIONS**

ARM2 (VTI-VY86C010)—Minimal design. 25,000 transistors, 6/12-MHz clock, 84-pin PLCC. Consumes 0.1W. Peak performance 6 native MIPS.

ARM3 (VTI-VY86C020)—310,000 transistors; 4-kbyte, 64-way set-associative cache. Consumes 0.5W, delivers 15 native MIPS. 144-pin FPGA, 160-pin QFP.

ARM6 (VTI-VY86C6)—Static core, also available as ASIC core. 34,000 transistors; 106×165-mm die.

ARM60/61 (VTI-VY86C060/61)—ARM6 core with JTAG port. 26- or 32-bit ext bus, 100-pin QFP, 84-pin PLCC.

ARM600/610 (VTI-VY86C600/610)—ARM6 core, JTAG port, 4-kbyte cache, MMU, write buffer, 160-pin QFP (600), 144-pin QFP. 610 has no coprocessor interface.

ARM250 (Plessey)—ARM2aS core with DRAM/ROM controller; SVGA/VGA/CGA video-display controller; I/O controller with serial, parallel, and PC interfaces. Video controller includes palette, video and sound DACs.

Support chips—VY86C110 memory controller, VY86C310 video/sound interface, VY86C410 I/O controller.

SUPPORT

□ **HARDWARE** The Platform Independent Evaluation card for ARM chips links to a development host via an RS-232C port. The card includes a boot module that links to a host debugger. Running on a Sun SPARCstation II, the instruction-set simulator executes ARM instructions at 0.25 MIPS. You can single-step ARM6-based μPs by manipulating the CPU clock.

□ **SOFTWARE** Cross-development tools are available for PCs, Macintoshes, and Sun workstations. These tools include a C compiler, assembler/linker, library with stand-alone runtime kernel, debugger, and instruction-set simulator. The C compiler conforms to the ANSI C standard and the Unix pcc (portable C compiler) conventions.

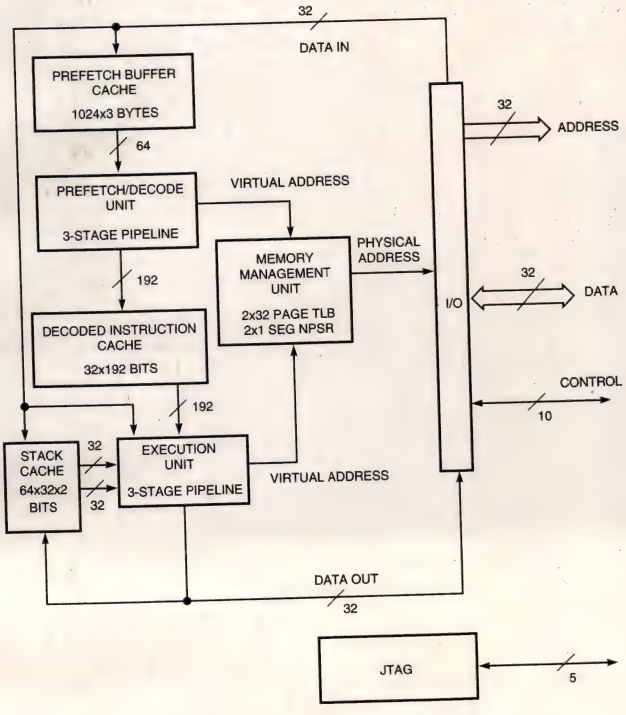
AT&T Hobbit

- 32-bit RISC C machine
- Stack architecture, no visible reg stack
- 34 variable-length instr
- 512-byte stack cache
- 3-kbyte instr cache (encoded), 3-way set associative
- 32-instr entry cache (fixed length, decoded)
- MMU with 2 32-entry TLBs
- 32-bit, nonmultiplexed synchronous ext buses
- Branch folding, static branch prediction
- 25-MHz clock
- 1-cycle execution for most instr
- 1.8 to 2.1 cycles/instr
- 15.5 VAX MIPS (20 MHz)
- 20-clock MPY; 38-clock DIV
- 4-clock min call overhead
- 2-clock ext bus R/W
- 2- or 4-word block transfers on ext bus (2,1 or 2,1,1,1)
- 800-nsec intr latency (12 to 20 clock ticks)

☐ **OVERVIEW** The 32-bit Hobbit is the result of almost a decade's worth of AT&T research toward building the ideal C machine—a CPU that efficiently executes C-language code. A stack machine, the Hobbit uses a stack cache to hold the C-generated stack for code execution. The CPU's minimal architecture delivers performance equivalent to first-generation, commercial RISC CPUs, but the Hobbit and its supporting chip set target a different market: handheld, portable applications, such as personal communicators. The chips are low-power devices that handle both 3.3 and 5V. The Hobbit CPU runs at 25 MHz. The four support chips include a system manager with power-management functions, a display controller, a PCMCIA controller, and a peripheral controller for a private P-ISA 16-bit bus. AT&T introduced the Hobbit and its supporting chip set in late 1992.

☐ **VENDORS/PRICING** AT&T Microelectronics developed the Hobbit and is the sole source. The Hobbit CPU—the ATT92010—sells for $35 each; the CPU with the chip set (less the P-ISA interface device) sells for approximately $100 (10,000).

ARCHITECTURE



The Hobbit's unique architecture delivers 32-bit, first-generation RISC performance. A stack-based machine, the Hobbit has no user-addressable registers. Instead, the CPU caches the application stack—the stack that C compilers create for functions' local values. The top of this stack is cached on-chip, but the CPU addresses the stack as memory, not as registers. Actually, the Hobbit is optimized for executing C programs and uses this stack as an alternative to CPU registers.

Instead of moving the stack into registers for fast code access, the Hobbit directly accesses it. The CPU caches the top of the application stack in a 256-byte stack cache. When a function is called, the hardware fills the stack with the function's activation environment. Hardware pops the environment when control returns back to the calling function.

Unlike classical stacks, user code can't push or pop data onto the application stack. However, you can achieve efficient stack usage by using stack instructions to ensure enough room on the stack for a function. The top of the stack cache also serves as a fast accumulator for interim results. According to AT&T, this 256-byte stack cache has a 87% hit ratio.

The Hobbit is actually two separate machines: a fetch/decode machine and an execution unit. The fetch/decode machine has a prefetch buffer (instruction cache) of 3 kbytes and a 3-stage, pipelined prefetch/decode unit. The fetch/decode machine tries to fetch, cache, and decode instructions before they are needed for execution. The decoded instructions are converted into 192-bit control words. The control words are held in a 32-entry decoded-instruction cache, which feeds instructions to the execution unit as needed.

Unlike most RISC processors, the Hobbit uses variable-length instructions that are fetched, decoded early, and then converted into fixed-length microcode-like control words for fast execution. Thus, the CPU has the benefits of both variable-length instructions for compact code and fixed-length instructions for faster execution.

If a branch follows an instruction, the branch is included (folded) into the leading instruction's decoded control word. In effect, branches are folded into the preceding instruction, compacting execution code. Each instruction control word has two address fields and a branch-prediction bit (set by the compiler) to preselect the path. Successfully predicted branches take one pipeline cycle in the execution unit; unpredicted branches take three cycles.

The CPU has a shallow, 3-stage pipelined execution unit and an MMU for memory protection and virtual-to-physical address translation. The MMU has two 32-entry TLBs, one each for data and instructions.

Mode	Current	Voltage (V)	Clock (MHz)
Normal	180 mA	5	20
Normal	50 mA	3.3	20
Standby	50 μA	5	0

In 132-pin QFP.

PERIPHERALS

ATT92011 system-management device—Functions include clock generation, intr routing, bus-master arbitration. Has DRAM and power controllers and serial I/O channel. Low power: 90 mW at 3.3V, 290 mW at 5V, 50 mW in standby mode.

ATT92014 display controller—Interfaces μP bus to display memory and display. Displays can be CRTs (to 1024×768 pixels×4) or color LCDs. Interfaces to VRAM or DRAM display memory. Low power: 75 mW at 3.3V, 230 mW at 5V, 50 mW in standby mode.

ATT92012 PCMCIA controller—Interfaces up to 3 PCMCIA devices to μP bus. Provides block moves and card-insertion intr. Low power: 50 mW at 3.3V, 130 mW at 5V, 50 mW in standby mode.

ATT92013 peripheral controller—Interfaces μP bus to private P-ISA 16-bit bus, which has some PX/AT bus characteristics. Handles up to 8 P-ISA devices/cards; provides 4 DMA channels between CPU and P-ISA buses. Low power: 50 mW at 3.3V, 130 mW at 5V, 50 μW in standby mode.

SUPPORT

☐ **HARDWARE** AT&T supplies a development system for the Hobbit that includes a PC/AT board with a 20-MHz ATT92010 Hobbit processor, 8 Mbytes of DRAM, and a 128-kbyte SRAM cache. The board runs with a Windows-based debugger. It can act as an ISA-bus master and can respond to as many as 6 individually jumpered backplane interrupts. The Hobbit and support chips all have a built-in JTAG port.

☐ **SOFTWARE** The Hobbit runs the PenPoint operating system from Go Corp (Foster City, CA). This object-oriented OS lets users draw inputs and use interactive graphics and was designed for portable applications. The Hobbit hardware can also run Unix, but Unix is not available for it. The development system has a Windows-based symbolic debugger. An assembler and compiler are available from Metaware (Santa Cruz, CA).

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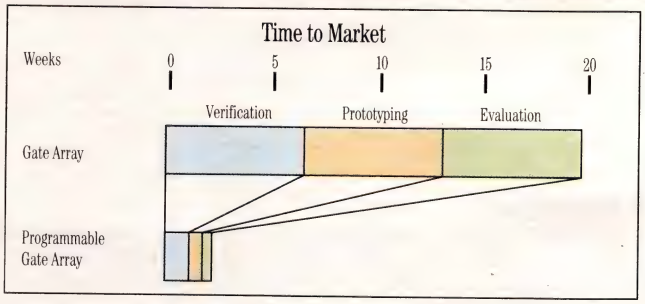

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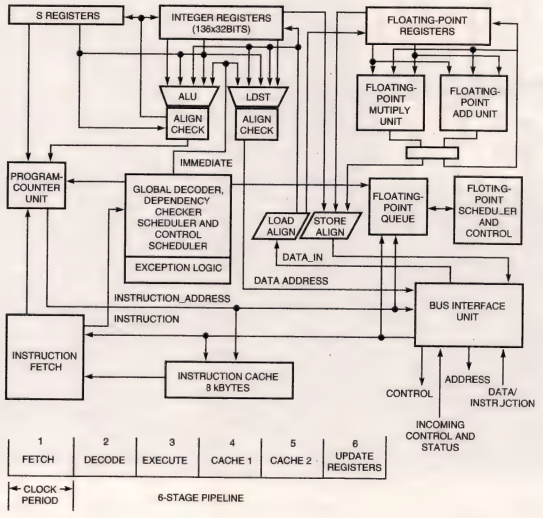
☐ **OVERVIEW** Cypress's Ross Technology subsidiary took the SPARC architecture in a new direction with the hyperSPARC, its 32-bit superscalar RISC SPARC μP. Unlike most RISC chips, the hyperSPARC is designed for implementation in an MBus module. The module plugs into the Sun workstation/server main memory or an MBus and lets users easily upgrade their systems. Unlike many superscalar RISC chips, the hyperSPARC runs with fast, tightly coupled off-chip caches, also in the MBus module. The μP has an 8-kbyte on-chip instruction cache, but its performance relies on up to 256 bytes of unified MBus cache controlled by a CY7C625 cache controller. The controller also serves as the module's interface to the MBus and can handle symmetric multiprocessing. The hyperSPARC CPU, cache controller, and cache chips interconnect via an Intra Module bus, which runs at the CPU clock rate. The CPU has a 5-stage pipeline that handles off-chip cache accesses by pipelining the cache. Clock rates range from 50 to 80 MHz; the hyperSPARC delivers 62-SPECint92, 64-SPECfp92 performance at 66 MHz.

☐ **VENDORS/PRICING** Cypress is the developer and sole supplier of the hyperSPARC. Samples will be available to SPARC International Executive members in 4Q92. The CYM221K module's sample price is $3500. (Module includes 55-MHz hyperSPARC CY7C620 CPU, CY7C625 cache controller, and 128-kbyte SRAM.)

Cypress hyperSPARC

- 32-bit SPARC RISC μP; 136 regs, on-chip FPU
- 1.1M transistors
- Superscalar
- 5-stage pipeline
- 8-kbyte, 2-way set-associative on-chip instr cache
- 128/256-byte ext cache with controller
- 32-bit addr, 64-bit data Intra Module bus
- FPU functional units: integer, branch, call, load/store
- Branch prediction
- MBus module: 1 or 2 CPUs, controller, caches
- Performance with 66.7-MHz clock and 256-kbyte off-chip cache:
- 62 SPECint92; 64 SPECfp92
- 0.9 cycles/instr; 133 native MIPS pk
- 1-clock execution (pipelined); issues 2 instr/cycle
- 17-clock MPY; 33-clock DIV
- 3-clock MPY, 14-clock DIV double-precision, floating-point ops
- 1-clock off-chip-cache R/W
- 32-byte ext-cache bursts
- Cache controller synchronizes chip clock, MBus; 20W dissipation max
- 3.3V signals for Intra Module bus

ARCHITECTURE



Cypress's hyperSPARC takes an unusual path to superscalar performance. Instead of beefing up on-chip caches, Ross Technology Div engineers opted to boost performance by relying on a small on-chip instruction cache and a large, unified off-chip cache with its own cache controller. Moreover, the hyperSPARC is only available in an MBus module, ready to drop into a SPARC system. The MBus is the standard SPARC system bus—a multiplexed, synchronous bus with 36-bit addresses and 64-bit data. MBus modules offer users an easy way to upgrade their systems and provide a tightly controlled environment for CPU and cache layout. MBus modules can hold multiple CPUs, and the MBus Level 2 spec defines using multiple masters for multiprocessing.

The hyperSPARC follows version 8 of the SPARC ISA spec. Operations center on a multiported register file, which holds 8 global registers and 8 overlapping register windows. There are 136 32-bit registers in the file. The hyperSPARC's separate FPU brings floating-point operations on chip. The FPU has its own instruction scheduler, instruction queue, pipelined multiply and add functional units, and 16 64-bit registers.

The CPU has a 5-stage pipeline and can issue up to 2 instructions per clock cycle. The on-chip 8-kbyte, 5-way set-associative instruction cache has a 32-byte (4-word) line size. An off-chip, unified cache of 128 or 256 kbytes of SRAM backs up the CPU. The Intra Module bus links the CPU to the cache controller and fast SRAM cache. The cache controller acts as an MMU with a 64-entry TLB by translating 32-bit virtual addresses to 36-bit physical addresses. Because the cache controller interfaces to the MBus, it acts as a bridge between the CPU and the system MBus, synchronizing operations between the CPU clock and the 40-MHz MBus clock.

The hyperSPARC pipeline drives four functional units, which can execute in parallel. The units are branch/call, integer, load/store, and an FPU. The FPU has its own scheduler and instruction queue. Floating-point instructions are queued and issued to the floating-point add or multiply functional units. These floating-point units are pipelined and can accept a new instruction each cycle.

To minimize branch delays, the hyperSPARC relies on a branch-taken prediction algorithm. All branches are assumed to be taken, and the hardware fetches the branch-target instruction pair next for execution. If the branch is not taken, there is a 2-cycle penalty. This algorithm works well for loops, where the most branches are taken except for the last iteration.

MBus—40-MHz, 64-bit synchronous, multiplexed bus used as main or system bus for SPARCstation 10s and SPARCserve 600s. Has 100-pin standard, double-row connector. Level 2 MBus spec adds 4 operations and 2 signals for shared-memory multiprocessing. You can hang system memory and secondary cache off MBus with controllers that interface to the bus. MBus is supplemented by SBus, a 25-MHz synchronous I/O or mezzanine bus for small peripheral and function cards.

Multiprocessing—Level 2 MBus spec defines using multiple masters and arbitration, allows for shared-memory multiprocessor signals and transactions. Also defines the MOSEI cache-coherency protocol for multiprocessing.

☐ VARIATIONS

CY7C620—Superscalar SPARC CPU, issues up to 2 instr/cycle. Meets SPARC ISA version 8.

CY7C625 cache-controller/memory-tag unit—Cache tags, clock synchronizer (CPU to MBus), tag memory (virtual indexed, physically tagged for snooping). Implements write-through, copy-back protocols.

CYM6221/4 MBus module—CPU, cache controller, 128/256 kbytes SRAM.

CYM6222/6K MBus module—2 CPUs, 2 cache controllers, 128/256 kbytes SRAM per CPU.

CY7C627 cache data unit—64-kbyte (16k×32-bit) SRAM with write-buffer pipeline and latched inputs, outputs. Needs no glue logic.

CY7C600 SPARCset—MBus SPARC chip set for MBus SuperSPARC or hyperSPARC modules. 7 chips including SBus controller.

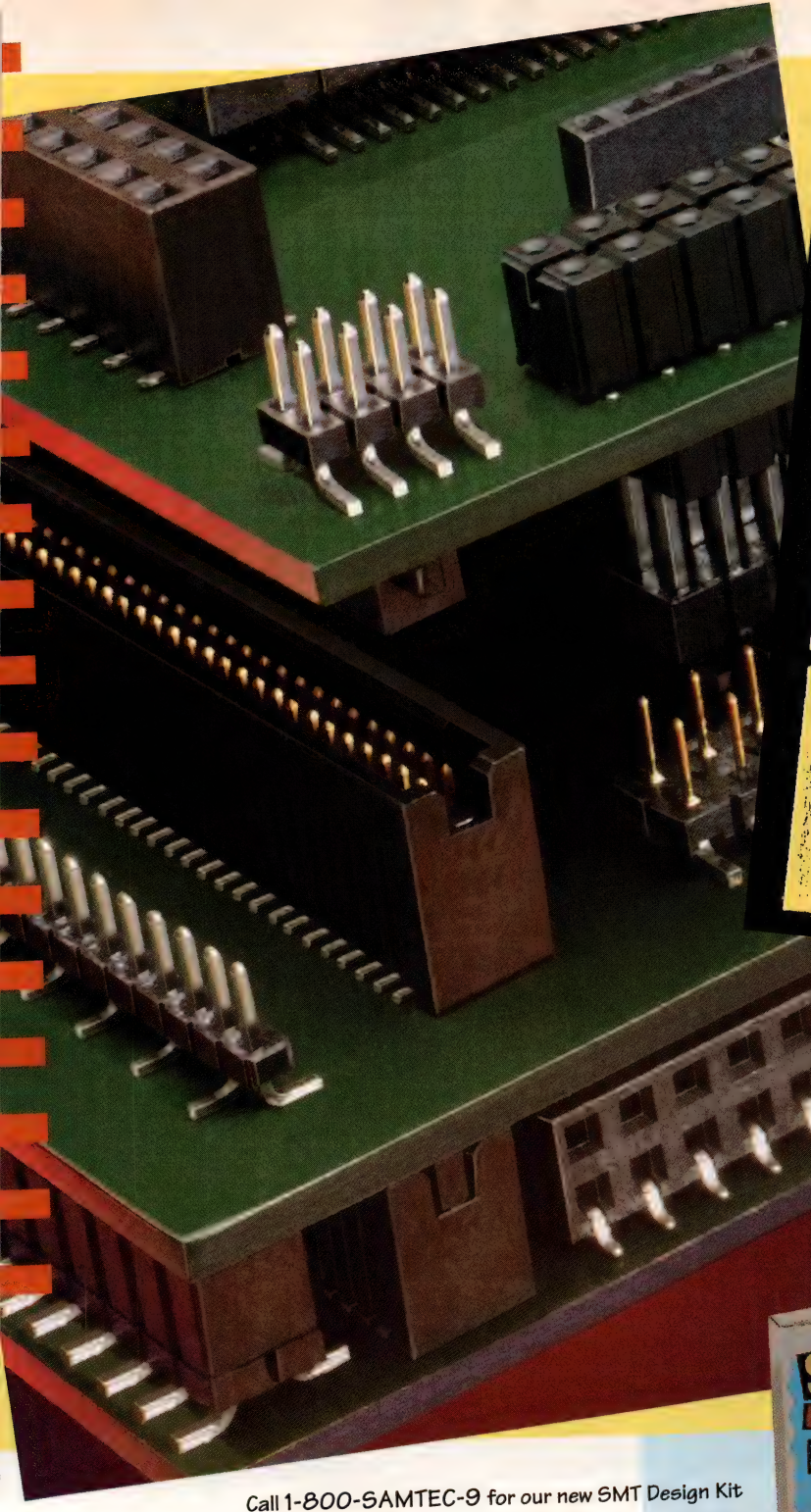
Nimbus SPARC board set—Includes ready-for-insertion board and Cypress SPARCset chips for SPARCstation clones.

MBus module	Current (max at 5V)	Clock (MHz)
CY7M6221K	4.8A	66.7
CY7M6222K	9.6A	66.7

SUPPORT

☐ **HARDWARE** An ICE is available from Embedded Performance (Santa Clara, CA) and logic analyzers from Biomation (Cupertino, CA) and HP's Colorado Springs Div. Cypress sells hyperSPARC evaluation boards. Nimbus Technology provides a ready-for-insertion board and chip set (CY7C600) for SPARCstation clones, and at least three vendors supply VMEbus boards carrying the hyperSPARC CPU.

☐ **SOFTWARE** The hyperSPARC complies with the SPARC ISA, version 8 spec. The processor runs a huge base of operating and application software including the SunSoft Solaris 1.0.1 OS, a Unix operating system. Also ported to the hyperSPARC are some real-time operating kernels for embedded operation. Ross Technology supplies boot/initialization software for the hyperSPARC and CY7C600 chip set.



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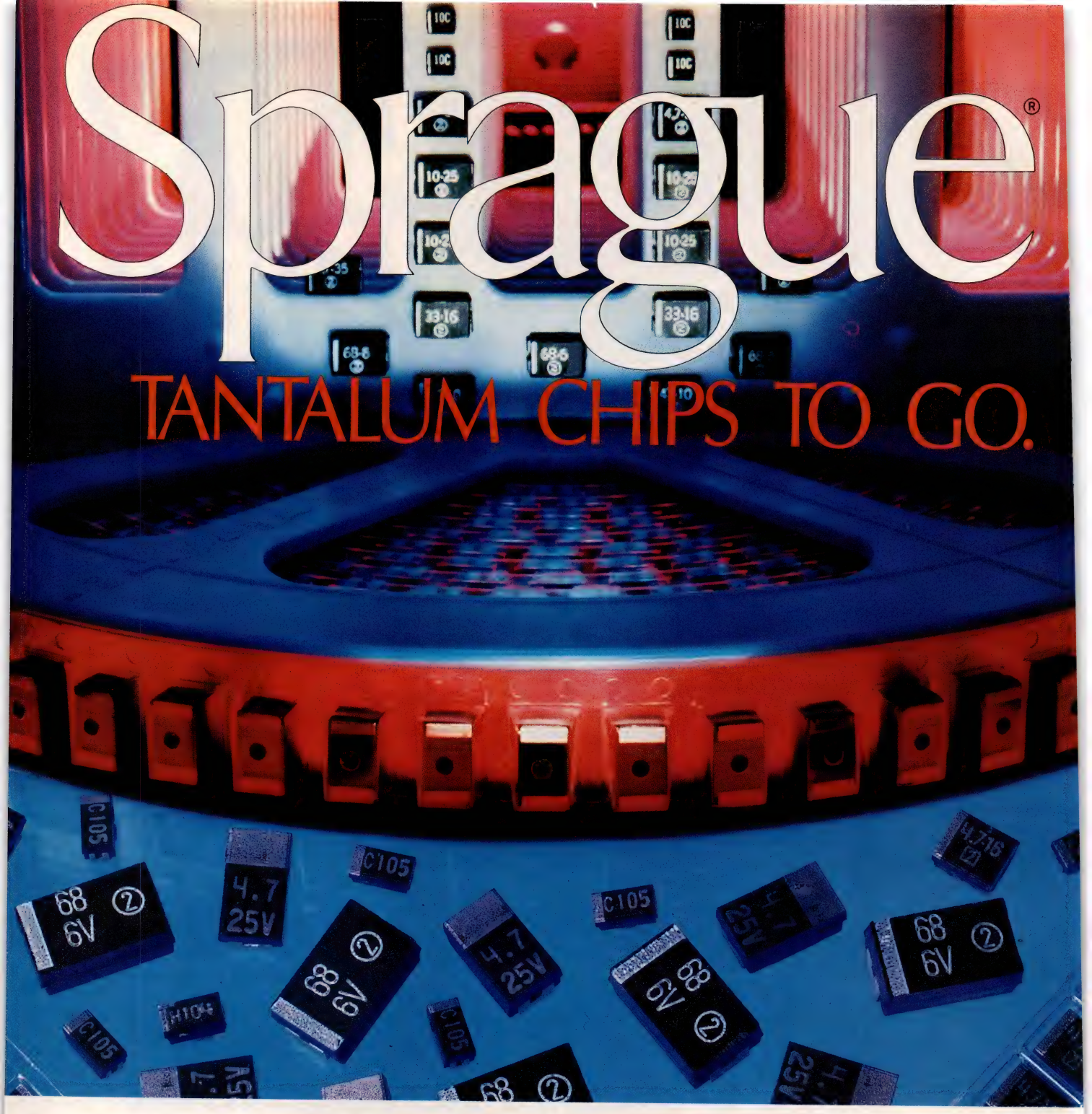

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CIRCLE NO. 40

☐ **OVERVIEW** The SPARC RISC architecture targets workstation and server computing. Fujitsu, the first SPARC vendor, has reworked the SPARC design for embedded systems. Fujitsu's SPARClite family adds on-chip data and program caches, a cleaner memory interface, timers, UARTs, an interrupt controller, and a debug unit. Currently, the SPARClite is the only single-chip SPARC μP with on-chip cache dedicated to embedded-system applications. Phillips/Signetics and other vendors are working on embedded SPARC processors, and SPARC vendors including Cypress and LSI Logic have built stripped-down SPARC CPUs that use support chips. The SPARClite family builds on a static SPARC core having a 32-bit ALU and a register file made up of 104 or 136 registers organized into 8 global registers and 6 or 8 overlapping register windows. The family has no on-chip FPU or FPU coprocessor interface.

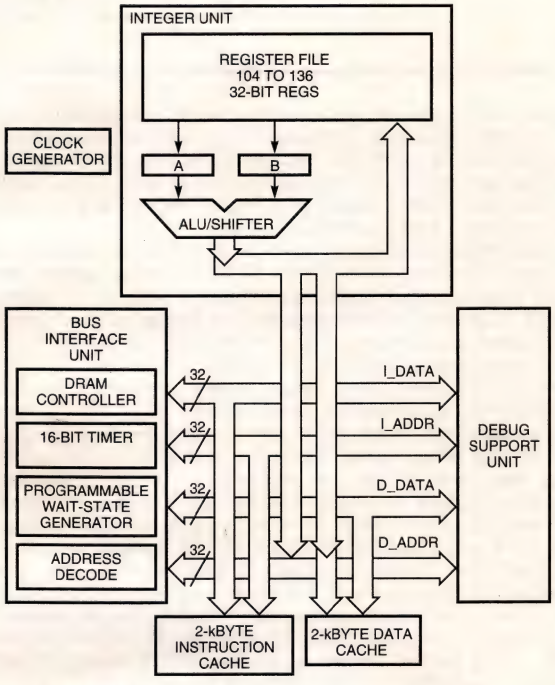
☐ **VENDORS/PRICING** Fujitsu is the developer and sole supplier of SPARClite μPs.

MB86930 (20 MHz, 208-pin QFP), $43; MB86931 (20 MHz, 256-pin QFP), $62; MB86933 (20 MHz, 160-pin QFP), $27.

Fujitsu SPARClite

- 32-bit SPARC μP; 104 or 136 regs, 6 or 8 reg windows
- 500,000 transistors
- 75 instr (version 8 ISA)
- 5-stage pipeline
- Up to 8 kbytes instr cache, 2 kbytes data cache
- 36-entry TLB
- 16-bit auto-reload timer
- DRAM wait-state/refresh generator, addr decoder
- 32-bit nonmultiplexed ext bus
- 4-bit intr bus (15 intr)
- 20/30/40-MHz clock (static core)
- 1 instr/cycle execution (pipe lined)
- 1-clock R/W
- 5-clock MPY; no DIV
- 17 native MIPS sustained (20 MHz)
- 1.6 cycles/instr
- Debug breakpoint reg
- 75-nsec max intr latency (20 MHz)

ARCHITECTURE



SPARClite processors feature a 32-bit ALU with a register stack of 104 or 136 32-bit registers. The registers are arranged into six or eight overlapping register windows, one window for each subroutine. Eight registers are set aside to hold global values. The SPARClite implements the ISA version 8 specification, which includes a full multiply instruction (unlike earlier SPARCs) and a step divide. SPARClite processors have 75 basic instructions and a load/store architecture to minimize complexity. User and supervisor operating modes and a JTAG test-vector interface let you test the chips in and out of a system.

Fujitsu engineers extended the SPARC pipeline to 5 stages for the SPARClite: fetch, decode, execute, memory, and write-back. The memory stage was added to minimize the effects of load/store operations. It reduces a load/store to 1-cycle execution. The stage is idle for non-load/store operations.

Unlike early SPARC chips, most SPARClite μPs have on-chip caches to hold critical data and processing routines for faster operation. There are separate data and instruction caches. Cache sizes run from 2 to 8 kbytes of instruction cache and up to 2 kbytes of data cache. The caches are 2-way set associative and have 16-byte (4-word) cache lines. The lines can be locked on chip and not swapped out for critical code or data. Fujitsu engineers also added debug registers to hold data values or addresses for individual and range breakpoints.

SPARClites run with DRAM, SRAM, and ROM/EPROM. The memory interface handles page-mode DRAM for low-cost, high-speed access using a 32-byte burst mode. The memory interface includes a refresh generator for DRAMs, programmable wait states for slower memory, and programmable chip selects for memory banking. One chip, the MB86932, includes an MMU for memory protection and paging and a 16-entry TLB. Boot-up memory interfaces are programmable; SPARClite CPUs can boot-up from 8-, 16-, or 32-bit ROM/EPROM.

Register windows—6 or 8 overlapping reg windows speed procedure calls and intr processing. Multiple contexts can be present concurrently by limiting the number of regs for a task. Reg windows can be set for different sizes or partitions. Reg-window mechanism can be ignored, and software will see a set of 32 general-purpose, 32-bit regs.

Special instructions—Scan word looking for first changed bit or first 1 or 0; put PC in reg, jump; load/store double word, save/restore caller (uses reg windows); swap reg with memory; tagged add/sub (generates overflow if MSB 0 and 1 are not 0); generate trap from conditions.

Addressing modes—Simple load/store mode: addr=reg+reg or reg+sign-extended 13-bit immediate value. Big-endian alignment.

☐ **VARIATIONS**

MB86930—20/30/40 MHz, 2-kbyte instr cache, 2-kbyte data cache, 136 regs in 8 overlapping windows, DRAM interface, 16-bit timer, 208-pin QFP, 179-pin PGA.

MB86931—20 MHz, 2-kbyte instr cache, 2-kbyte data cache, 136 regs in 8 overlapping windows, DRAM interface, 16-bit timer, 2 USARTs, 4 16-bit counter/timers with prescalar and compare/capture reg, interrupt controller, 256-pin QFP.

MB86932—20/40 MHz, 8-kbyte instr cache, 2-kbyte data cache, 136 regs in 8 overlapping windows, 16-entry MMU, DRAM interface, 16-bit timer, memory burst mode, 2-channel DMA, 8/16/32-bit boot-up modes, 208-pin QFP.

MB86933—Stripped-down version, 20 MHz, no cache, 104 regs in 6 overlapping windows, DRAM interface, 16-bit timer, 8/16/32-bit boot-up modes, 160-pin QFP.

Chip (static)	Current (max)	Package	Clock (MHz)
MB86930	475 mA	208-pin QFP	30
MB86932	650 mA	208-pin QFP	40
MB86933	210 mA	160-pin QFP	20

Fujitsu's SPARClite is an embedded version of the standard SPARC processor. Unlike the original SPARC μPs, which required lots of support logic, SPARClite μPs minimize design-in time and require little glue logic. The chips have an on-chip, programmable DRAM interface that handles page-mode DRAM for fast, burst-mode accesses.

SUPPORT

☐ **HARDWARE** Most chips have a debug-support unit, which has 6 debug registers (2 code address, 2 data address, 2 data values). A 10-pin emulation bus for in-circuit testing is available. Fujitsu provides evaluation boards that link to a PC host for debugging.

☐ **SOFTWARE** Compatible with standard SPARC software. Most chips will not run Unix because they don't have an MMU. Compilers, development tools, and operating software are all available for the SPARClite.

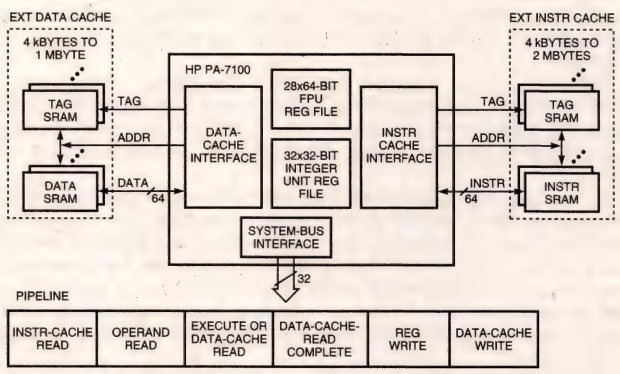
□ **OVERVIEW** HP pioneered RISC μPs with its PA-RISC architecture. A classic, early RISC μP, the PA-RISC has a load/store architecture with a fixed instruction word. The instruction set and addressing are relatively simple, and there is no hardware integer multiply or divide. The two PA-RISC chips—the PA-7000, which powers HP Snakes workstations and servers, and the PA-7100—deliver top-end RISC performance. The PA-7000 runs at 66 MHz and has up to 3 Mbytes of instruction and data cache feeding its Harvard architecture. It uses an FPU chip HP developed with Texas Instruments; the later PA-7100 moved the FPU on-chip. The superscalar PA-7100 runs at 100 MHz and delivers 80-SPECint92, 140-SPECfp92 performance. The PA-RISC is a proprietary architecture, but HP has opened the architecture to other companies by founding the Precision RISC Organization (PRO). Several super- and near-super computer vendors have committed to PA-RISC μPs, and work is ongoing on embedded PA-RISC chips.

□ **VENDORS/PRICING** Hewlett-Packard is the developer and currently the only source of PA-RISC chips. HP has licensed the architecture to chip vendors Hitachi and Oki. Additionally, HP is making the PA-7100 available to Precision RISC Organization (PRO) members as a part of a processor module with SRAM caches. OEM pricing is negotiable.

Hewlett-Packard PA-RISC

- Specs for PA-7100: 32 general regs, 28 floating-point regs
- On-chip FPU
- 155 instr
- 6-stage CPU pipeline
- 2 64-bit buses, on-chip cache controller
- Up to 2 Mbytes data, instr caches (ext)
- 32-bit system bus
- 32-bit physical, 48-bit virtual addr spaces
- Access protection
- Instr combine ALU operations and branches
- Specs for PA-7100: 66- to 100-MHz clock
- Issues up to 2 instr/clock: 1 CPU, 1 FPU
- 1-clock instr execution (pipelined)
- 80 SPECint92; 140 SPECfp92
- Integer MPY done in FPU
- 20-nsec floating-point MPY, ADD
- 10-nsec floating-point MPY, ADD (pipelined)
- 1-clock cache R; 2-clock cache W
- 1-cycle penalty for branch-prediction miss
- 200 Mflops peak (MPY and ACCUM ops)
- Uses 9-nsec SRAM at 100 MHz

ARCHITECTURE



□ **VARIATIONS**

PA-7000—CPU for 700 Snakes series workstations/servers. Static design has 577,000 transistors, external caches (data SRAM and cache-tag SRAM). CPU interfaces to TI's FPU and handles up to 2 Mbytes of data cache and 1 Mbyte of instruction cache. Has 5-stage pipeline, on-chip MMU with 2-kbyte pages, clock rate up to 66 MHz. 408-pin PGA.

PA-7100—Upgraded PA-7000 CPU. Has 850,000 transistors, on-chip FPU, clock rate to 100 MHz, longer 6-stage pipeline, and on-chip unified MMU with 4-kbyte pages. 508-pin PGA.

PA-7100 module—Drop-in module eases designing in chip as clock rates climb. Runs CPU at multiple of module-bus rate (1:1, 2:1, 3:2), handles module-bus rates up to 66 MHz. 12-layer, 4.1×4.4-in. module holds data and instruction SRAM caches up to 1 Mbyte for each. At 100-MHz CPU clock rate, cache sizes are restricted to 256 kbytes SRAM each.

PA7100

Current (max)	Voltage (V)	Clock (MHz)
2.9A	5	66
4.4A	5	100

In 504-pin static PGA.

A pioneering RISC μP, the HP PA-RISC was introduced in 1986 as the Spectrum architecture and was initially a TTL multichip implementation. The processor's many classic RISC features include a register-based architecture, 32-bit ixed instruction word, simple addressing modes, load/store operations, simple hard-wired instructions, and no full integer multiply or divide instructions.

A Harvard architecture, HP PA-RISC implementations treat data and instruction separately—each has its own interface to minimize stalls and maximize throughput. The latest PA-RISC chip—the PA-7100—runs with large external caches connected by a 64-bit, nonmultiplexed bus.

The PA-7100 integrates a floating-point unit with the CPU. The register-based operations center around the CPU's 32 32-bit general registers and the FPU's 28 64-bit floating-point registers. The μP issues up to two instructions per clock cycle: one CPU instruction and one floating-point instruction.

HP took a system-development tack with the PA-7000 and PA-7100. Engineers boosted performance by kicking CPU clock rates up to 100 MHz (66 MHz for the PA-7000) and adding large, separate instruction and data caches. Instead of trying to shoehorn caches onto the silicon, the engineers used HP's high-speed logic and board design capabilities to drive on-board caches at CPU clock rates. The PA-7100 can run its 64-bit-wide cache interfaces at 100 MHz for reads. Both chips handle up to 3 Mbytes of data and instruction cache and have an on-chip cache controller. The external caches are divided into cache data SRAMs and cache tag SRAMs (holds tag data). A separate 32-bit, multiplexed system bus links the CPU to main memory.

The combination of superscalar execution, 100-MHz clock rates, and large, fast external caches puts the PA-7100 based system at the head of the RISC power curve. Large caches minimize cache thrashing and the effects of multitasking on performance. In contrast, TI's superscalar SuperSPARC has the largest RISC on-chip caches: 36 kbytes. The SuperSPARC cache takes up 3.1M transistors; the PA-7100 has 850,000 total transistors.

The PA-7000 has a 5-stage pipeline; the PA-71000 extended the pipeline to 6 stages for a faster memory interface. The PA-7100 uses a combination of branch delays and branch prediction to minimize the effects of branches on program execution in the larger pipeline.

HP engineers tuned the PA-7100. The multiword instruction MOVE32 moves a 32-byte block between main memory and the CPU system I/O bus. A load to R0 (a null register) fills the cache line for the addressed data, putting data into the cache before it's needed to eliminate cache-miss penalties. To minimize code and speed execution, some instructions combine short branches with general operations.

Addressing/spaces—PA-RISC can use up to 64k 32-bit address spaces in a 48-bit virtual addr space. Resembling nonoverlapping segments, each space has its own base reg concatenated with a 32-bit offset. The PA-7100 has a 32-bit physical address space and 4 privilege levels.

Access protection—For secure operation, read/write/execute access is controlled at page level (4-kbyte pages). Four control regs hold protection IDs for the current process. IDs are matched against the addressed item's TLB-entry access ID. Access protection minimizes effects of wild pointers, accesses into code, and execution of data.

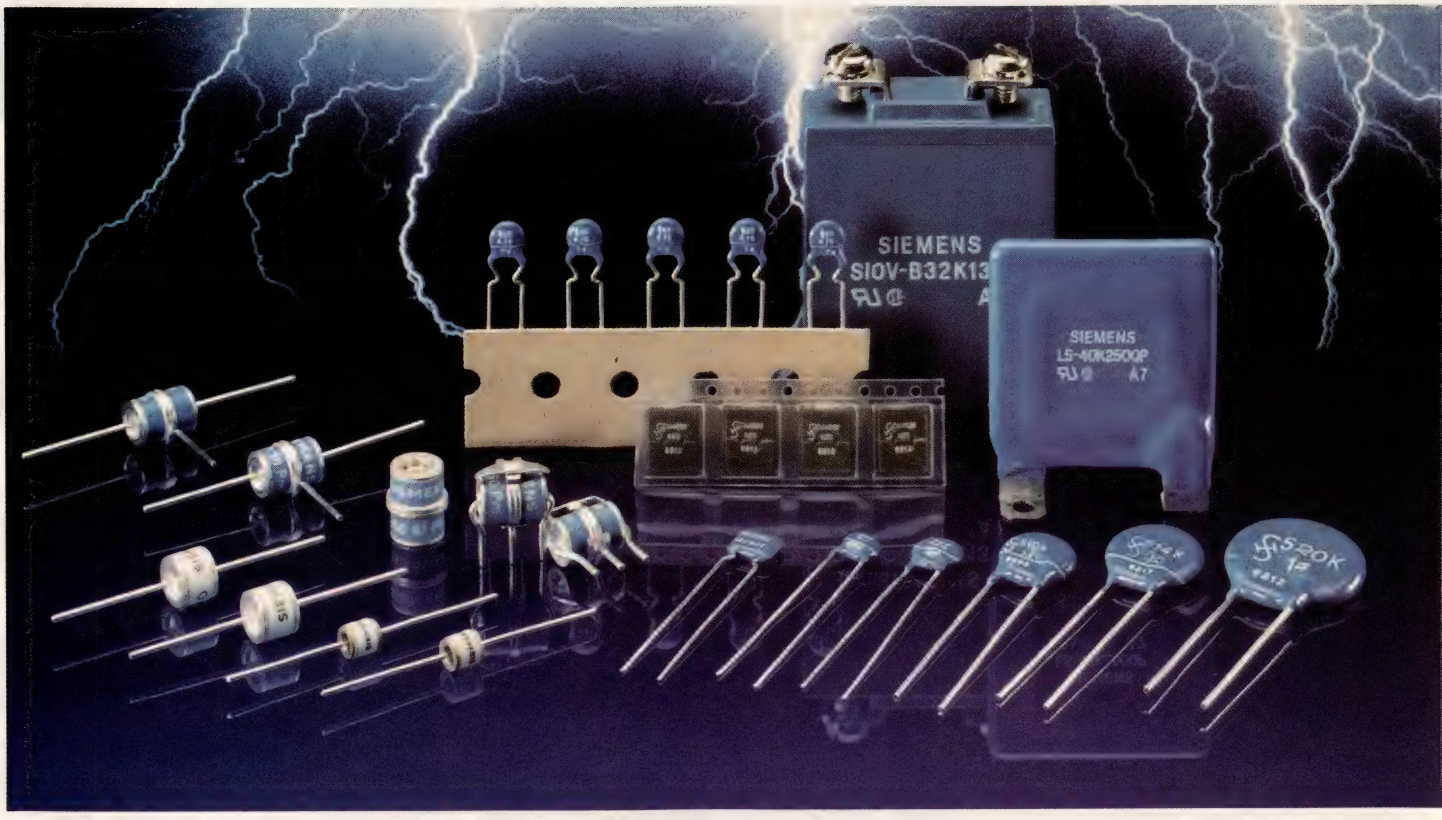
Nullification—Combines test-and-branch with most operations. If nullification bit is set and condition is false, skips next instr.

SUPPORT

□ **HARDWARE** Currently, no commercial hardware development tools exist for the HP PA-RISC architecture. All development work has been done at HP, which has developed in-house, specialized tools that are available to PRO members only. However, HP is pushing designing in the processor at a module level, which requires fewer development tools. The PA-7100 chip has built-in scan testing.

□ **SOFTWARE** HP pioneered RISC compilers and development software. A full set of HP PA-RISC development software runs on HP platforms. The HP PA-RISC runs HP-UX, a Unix-based operating system. Many applications have been ported to the architecture over the years and are available.

SIEMENS



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☐ **OVERVIEW** The 32-bit Hyperstone E1 μP is part of a new twist in microprocessor evolution. It combines both RISC and CISC technologies and targets low-power, high-performance embedded applications. Introduced in 1990, the Hyperstone's performance peaks at 40 native MIPS. At 33 MHz, the CPU can run with low-cost DRAMs. Based on a large register set, the CPU holds 19 global and 64 local registers. The local registers are arranged in a stack and have overlapping stack frames for parameter passing between functions. The CPU relies on a small 128-byte instruction cache to speed execution but has no data cache. Hyperstone instructions are made up of 1, 2, or 3 16-bit half words for compact code. A small chip, the Hyperstone has about 85,000 transistors.

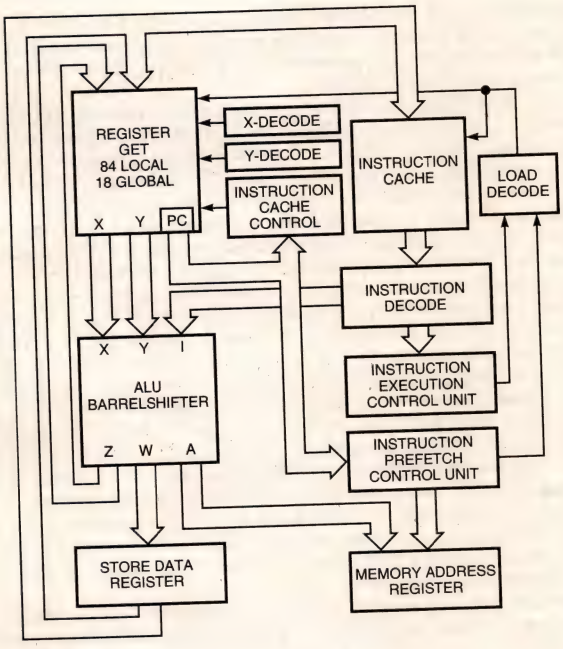
☐ **VENDORS/PRICING** Hyperstone Electronics is the developer of the Hyperstone architecture. Hyperstone processors are supplied by Hyperstone, Alps Electric Co Ltd, and Zilog, which also plans to use the CPU as an ASIC core.

Hyperstone E1, 25 MHz, $29; 30 MHz, $39; 40 MHz, $59.

Hyperstone E1

- 64 local, 19 global regs
- Circular reg stack with stack frames
- 85,000 transistors
- 188 instr
- 128-byte instr cache; no data cache, MMU
- 4-Gbyte addr space; 512-kbyte I/O addr space
- Nonmultiplexed ext buses: 30-bit addr, 32-bit data
- 32-bit timer with prescalar, compare reg
- DRAM controller for refresh, RAS-CAS multiplexing
- 1 ext intr
- Static, 20/25/40-MHz clock (divide-by-1 internal)
- 25-nsec NOP
- 50-nsec mem-reg ADD
- 25-nsec SHIFT
- 425-μsec MPY; 900-μsec DIV
- 75-nsec MPY-ACCUM
- 2-clock branch (taken); 1-clock branch delay; 1-clock branch not taken
- 1-clock DRAM R/W in page-mode bursts (5 clocks, first access)
- 4-clock R/W exchange

ARCHITECTURE



The Hyperstone E1 μP targets embedded systems. It is neither a classic RISC or CISC machine. Instead, it borrows from both design technologies to build a minimal processor that combines CISC silicon efficiencies with RISC-level performance.

Like a RISC CPU, the Hyperstone is register oriented. It's built around a register stack that holds 64 general-purpose and 19 global registers. The global registers are directly addressed and include an SP, PC, status, upper-stack bound, floating-point exception, and 14 general registers. The local registers are organized into a 64-word circular stack to hold function/subroutine activation environments. The stack crosses the register-memory boundary. Stack frames have up to 16 registers or words. Current stack frames are kept on-chip and are automatically pushed down to off-chip memory as the register stack fills up. Similarly, as the frames are popped off the stack, frames in memory are automatically passed to the on-chip stack.

The stack frames can overlap to share calling parameters between the called and calling functions. The CPU can address the current register frame directly as registers L0 to L15. The frame size is programmable via a 4-bit frame field in the status register. A frame-pointer field in the status register references the first register in the current register stack frame. This reference is relative to the 64-word circular register stack file.

Unlike RISC CPUs, the Hyperstone has variable-length instructions to minimize code space. The basic instruction word is 16 bits, but instructions can have one to three 16-bit half words, which permits 32-bit constants or addresses. Rather than traditional 3-operand RISC instructions, the Hyperstone uses two operands to further compress instruction length. The result of a 2-operand instruction returns to one of the operands, eliminating the need for a third.

A shallow 2-stage pipeline simplifies branch and exception processing. Branches can be standard or delayed. Standard branches use 2 cycles if the branch is taken (instruction in cache); delayed branches take 1 cycle. Both branch types use 1 cycle for a nontaken branch.

The Hyperstone uses a small 128-kbyte instruction cache but has no data cache. It also lacks floating-point and MMU units. Floating-point software routines are provided in a function library, and the CPU can use an external MMU. The FETCH instruction stops execution until n+1 instruction half words are prefetched into the cache, thus letting the CPU take in a burst of instruction half words without the interference of data fetches. FETCH sets up the cache with a string of ready-to-execute instructions without paying miss penalties for first-time access. Load, store, and exchange instructions are pipelined 2 deep at the external bus.

Stack frames—16 max; current frame kept in reg, others can be in memory. Upper stack bound is guarded. Automatic data transfer between memory and reg parts of stack.

Addressing modes—Absolute, reg indirect, reg indirect with post-increment, reg indirect with signed displacement, next addr (reg indirect with post-increment by constant), stack addr.

Special instructions—Exchange reg with memory, compare bits, move double word, test number of leading zeros, set conditions (store condition codes in reg), check addr upper bound, index move (check index for bounds and shift 1, 2, 4, or 8 bits), decrement frame pointer to include passed parameters then readjust frame length.

☐ **INTERFACES**

DRAM controller—Handles RAS-CAS (row address strobes, column address strobes) multiplexing; provides DRAM refresh signals, memory parity generation/checking. RAS precharge and CAS delay times are programmable (0 to 3 wait states). Refresh is also programmable; can be disabled or set to occur every 128, 256, or 512 cycles.

Address space—Partitioned into 4 spaces: DRAM, 2 ROM or SRAM, and 1 ROM. The 2 MSBs of an address—bits 31 and 30—select the addr space.

Bus—Hyperstone can function with multiple bus masters. Control can alternate between bus masters from cycle to cycle; 1-cycle cost to switch masters. Programmable bus timing for all I/O devices.

Current (max)	Voltage (V)	Clock (MHz)
210 mA	5	20
250 μA	5	25

In 144-pin PGA, 120-pin QFP.

SUPPORT

☐ **HARDWARE** Hyperstone provides an evaluation board for the Hyperstone E1 μP. The board includes a 25-MHz CPU, 1 Mbyte of DRAM, up to 256 kbytes of EPROM, and a serial UART that links to a PC development host. A ROM debug monitor is available for board-level debugging.

☐ **SOFTWARE** Hyperstone furnishes a macro assembler, C compiler, and window-oriented source-code debugger. The C compiler handles ROMable code and fills the delay branch slot where possible. A real-time operating-system kernel is also available for the Hyperstone CPU.

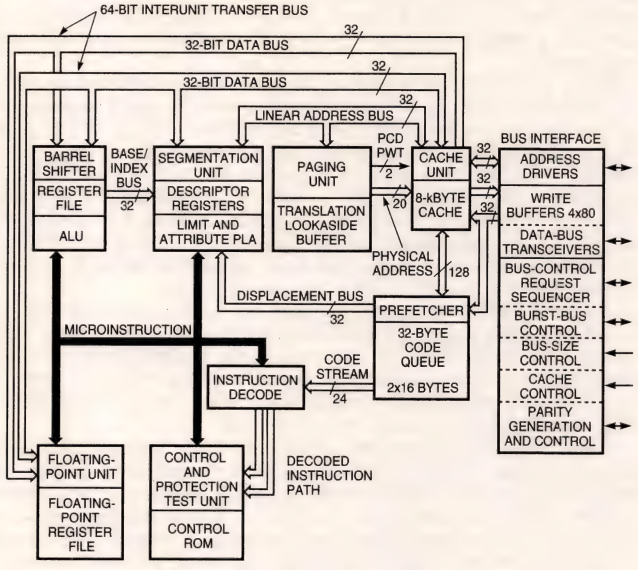
Intel 80386/80486

- 80386: 32-bit μP, 80387 math coprocessor
- 80486: 32-bit μP, 8-kbyte cache, on-chip FPU
- 32-bit regs: 4 general, 4 index/pointer
- 6 16-bit segment regs
- 32-bit addr space; paged, segmented addr
- Segment, tasking protection with 4 privilege levels
- 8086 real mode
- 32-bit nonmultiplexed ext bus
- Power-management features; 3V versions
- 4 breakpoints via 4 on-chip debug regs (486)
- Up to 40-MHz 386 clock (divide-by-2 internal)
- Up to 50-MHz 486 clock (ext and int); up to 66 MHz for clock-doubler versions
- 1-clock reg-reg ADD, NOP (486)
- 2-clock reg-reg ADD, 7-clock reg-mem ADD (386 internal clock)
- 42-clock MPY; 40-clock DIV (486)
- 2-clock R; 4-clock W (386, internal clock)
- 2-clock R/W, 1 clock for burst mode (486)
- 107-clock intr latency (486)

□ **OVERVIEW** Thirty-two-bit 80366 and 80486 microprocessors dominate desktop computing, driving more than 20 million PCs. The Intel-developed architecture is based on the earlier 16-bit 8086/8088, which powered the first IBM PC. In 1985, Intel's i386 brought 32-bit processing to IBM PCs. The i486 followed in 1989 and added RISC-like simple instructions, on-chip caches, and an on-chip FPU for higher performance. Intel's corner on 386/486 chips ended in 1990 when vendors including AMD, Chips & Technologies, and Cyrix began producing 386s and, later, 486s. Consequently, prices have fallen dramatically. New 386/486 versions target portable applications by featuring higher integration, lower power, and power-management features. Intel's "clock-doubler" 486s double the input clock rate—a 33-MHz board runs a 66-MHz CPU. Cyrix 486s match 386SX or DX pinouts with a 486 ISA (Industry Standard Architecture) and a small cache. AMD, C&T, and Cyrix have added power-management features to their 386/486s, as did Intel with its 386SL.

□ **VENDORS** Intel developed the 80386/80486 architecture. Advanced Micro Devices and Chips & Technologies developed their own 386 ISA-compatible implementations. Cyrix implemented a low-power 486 on a 386SL, DX pinout; Texas Instruments is a second source for the Cyrix chips.

ARCHITECTURE



Register-based, the 80386/486 doesn't provide the classic set of general-purpose registers. Instead, the architecture has four general-purpose and four index/pointer registers, supplemented by six 16-bit segment registers and two 32-bit status and control registers.

Intel's 8086 designers used segments to extend addressing to 1 Mbyte. By shifting the 16-bit segment register 4 bits to the left, they generated a 20-bit address. Addressing is relative to the segment base, displacements are added to the shifted base, and segments are limited to 64 kbytes. The 80386/486 also uses this mechanism. However, because the registers are now 32 bits, the segment limits are extended to the full 4-Gbyaddressing range, and the segment register references a segment descriptor with a 32-bit base address. These descriptors also carry addressing-range and protection limits.

Intel designers have continually added system-level functions to their processor designs. The 386, for example, pioneered on-chip debug registers for breakpoints and debugging. And starting with the 286, Intel engineers built in system-level protection by adding four privilege levels of access protection. Hardware prevents data accesses into code, data being executed as code, and access to inner privilege levels by outer levels.

Software developers are starting to use the 386/486's protected-mode privilege-level features. For example, OS/2 relies on privilege levels to create a more fail-safe runtime system. Hardware descriptor registers hold segment-access rights along with segment base-address and size limits. In protected-mode addressing, a 16-bit selector points to a segment descriptor, which furnishes a base address. The base address is added to the 32-bit effective address to produce a 32-bit linear address, which is then used as a physical address or as a linear-page address.

The 486 combines the 386 architecture with a RISC-like, pipelined implementation for basic instructions, an 8-kbyte unified cache (both data and code), and an on-chip math or floating-point unit. To speed execution, the 486 prefetches four 32-bit words at a time and holds up to 32 bytes in a byte code queue. Instruction lengths range from 2 to 17 bytes.

The 386 divides the external clock by 2, halving internal frequency; the 486 runs at the external clock rate. The 486 trimmed the 386's basic memory cycle from 4 to 2 clocks. The 486 also added a burst mode, which lets it move up to 4 words per burst (2-1-1-1). The 386 has two modes: real mode, which limits execution to the 8086's 1-Mbyte memory; and protected mode. The 486 adds another mode—virtual 8086 mode—which provides a virtual 8086 with protected-mode checks.

AMD developed its own static version of the 386 using 80386 microcode and has announced (but has yet to ship) a 486. Cyrix took a different tack. It implemented the 486 ISA for 386 portable applications by using 16-bit 386SX and 32-bit 386SL pinouts in a static design. The chips have a small 1-kbyte cache to boost performance. Chips & Technologies has two 386 implementations, one with a 512-byte on-chip cache.

Stack—Stacks reside in memory, use 3 regs: stack-segment register, SP, and stack-frame base pointer. These regs are part of the reg set but are dedicated to stack operations.

Clock-doubler 486s—Later 486s have clock-doubler versions. These chips use a PLL to double the system clock and use the doubled clock to drive the processor. As long as the CPU executes out of the 8-kbyte cache, performance is doubled; otherwise, cache misses degrade performance.

□ VARIATIONS/PRICING

Vendor	μP (speed in MHz)	Price (1000)	Comments
AMD	386DX (25/33/40)	$53	Standard 386, QFP/PGA.
	386SX (20, 25)	$47/$42	386 with 16-bit bus, QFP.
	386SXLV (20, 25)	$43	3V 386SX, 16-bit external bus, QFP.
	386DXLV (25)	$61	3V standard 386, QFP.
C&T	308600DX (33)	$75	Redesigned 386, 10% faster than standard 386.
	38605DX (33)	$80	Redesigned 386, 512-byte cache, power-management features.
Cyrix	486DLC (25/40)	$116/$146	486 ISA, 386DX pinout; FPU coprocessor available.
	486SLC (25/33)	$99	3V 486 ISA, 386SL pinout; 16-bit bus, 1-kbyte cache.
Intel	386DX (25/33)	$89/$102	Standard 386, QFP.
	386SX (16/25)	$43/$67	386, 16-bit bus, power-management features, QFP.
	386SL (16/20/25)	$48/$67/ $96	Redesigned 3.3V 386SX; power management, cache controller with tags.
	486SX (16/33)	$94/$189	486, 16-bit bus, no FPU, QFP.
	486SX (25/33)	$113/$132	3.3V 486SX; 16-bit bus, no FPU, QFP.
	486DX (33/50)	$328/$502	Standard 486, on-chip FPU.
	486DX2 (50/66)	$457/$600	Clock-doubler 486; 25-MHz clock, 8-kbyte cache.
	486SL (25)	$269	3.3V 486; DRAM, ISA bus controllers; 32-bit bus; QFP.

SUPPORT

□ **SOFTWARE** The 386 and 486 have a huge development and application software base. However, the bulk of this software, including most compilers, is written for 16-bit operations. Thirty-two-bit compilers are now available, including a C compiler from Intel. Almost all languages have a compiler for the 386/486.

□ **HARDWARE** The 386 and 486 have 6 debug registers: 4 code/data breakpoint registers and 2 control registers. The breakpoint registers can be set with addresses for halting execution on a program or data access. A full set of hardware development tools, including ICEs and logic analyzers, is available for the processors.

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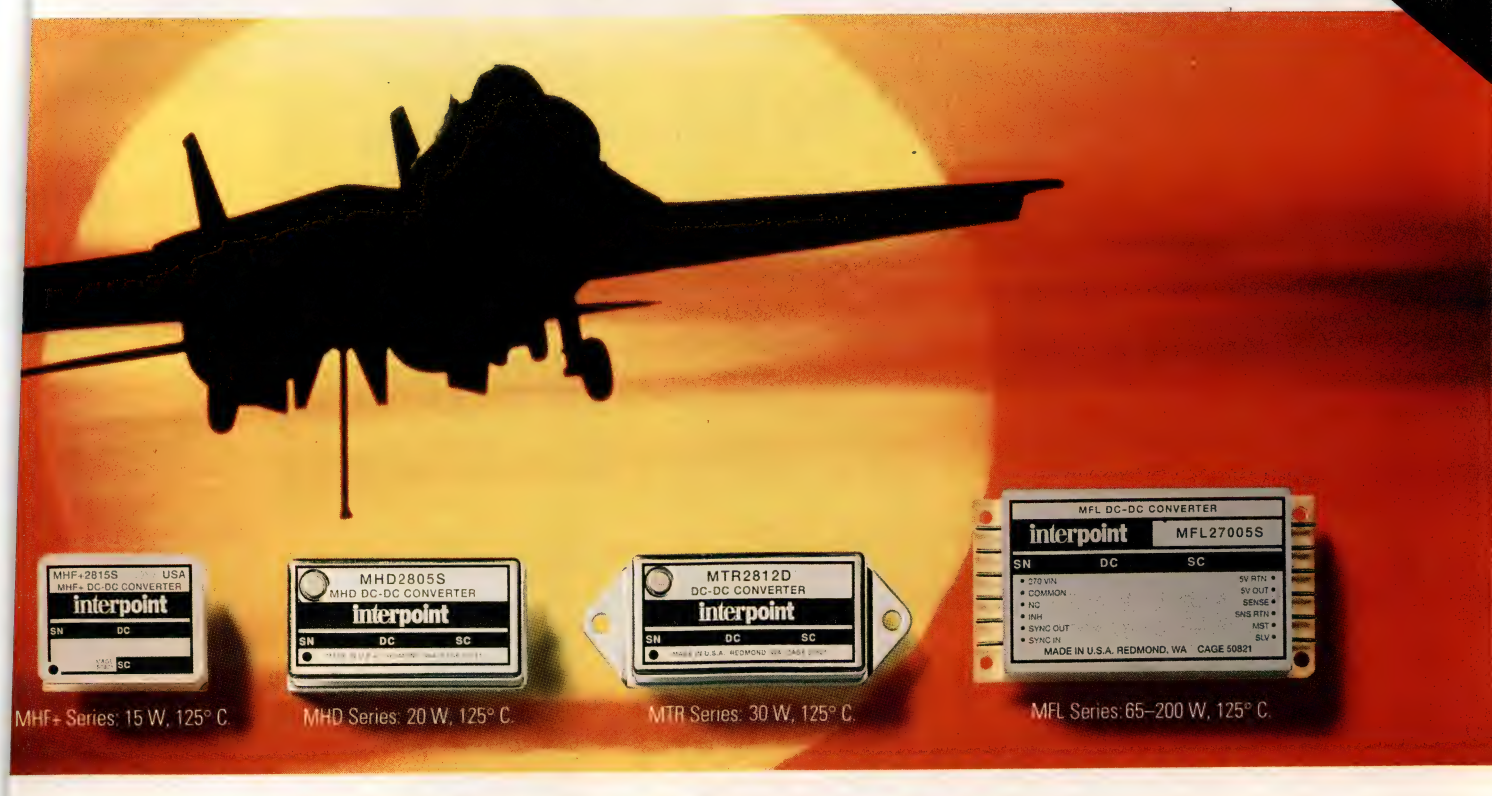

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CIRCLE NO. 46

32-bit μP

Intel i860

- Reg-based μP has 32 32-bit regs, 8 128-bit floating-point regs
- 32-bit CPU, 64-bit FPU, 64-bit graphics engine
- 90/94 instr (XR/XP)
- Pipelined functional units: 4-stage CPU; 3-stage floating-point multiplier, adder; 1-stage graphics unit
- 16-kbyte instr, data caches (XP); 4-way set associative, 32-byte lines
- Write-back/through cache, employs MESI cache-coherency protocol (XP)
- 64-bit ext memory bus
- 128-bit internal data paths to caches, FPU regs
- 25/33/40/50-MHz clock
- RISC VLIW architecture exe cutes CPU, FPU instr concurrently
- 1-cycle instr execution (pipelined)
- 20-nsec reg-reg ADD, NOP
- 40-nsec reg-mem ADD
- 32-byte burst-mode memory (XP)
- 1-cycle/stage floating-point ADD, MPY (single precision)
- 2-cycle/stage floating-point MPY (double precision)
- 60-nsec double-precision floating-point ADD and MPY
- 2-clock ext-memory R/W

□ OVERVIEW

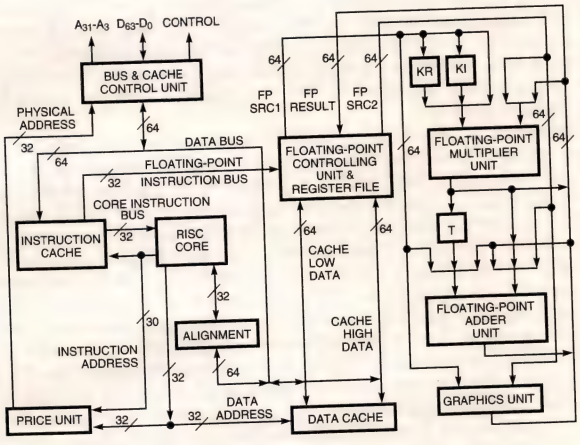
Introduced in 1989, Intel's 32-bit 80860 RISC μP initially targeted Unix workstations but found employment as a high-speed coprocessor, a graphics coprocessor, and a core for super and near-super computers. The 80860 is the core CPU of Intel's Touchstone multiprocessor. The i860 introduced several innovations for RISC-based microprocessors. It was the first RISC superscalar/VLIW processor: It can start up to two instructions per clock cycle—one CPU and one FPU instruction. Also, i860s integrated a 64-bit graphics unit on chip for pixel and Z-buffer processing. The register-based μP takes in 64 bits at a time from memory and has 128-bit-wide inner data paths to speed graphics and floating-point processing. There are two versions: the original i860XR with a 16-kbyte cache and the newer i860XP with a 32-kbyte cache and multiprocessing features.

□ VENDORS/PRICING

Intel developed the i860 and is the sole supplier.

80860XP: 40 MHz, $406; 50 MHz, $507. 80860XR: 25 MHz, $120; 33 MHz, $230; 40 MHz, $301 (1000, in PGAs).

ARCHITECTURE



□ INTERFACES

Memory—The XP MMU handles 80386/486-compatible 32-bit addressing. The external bus has a 32-bit address bus and a 64-bit data bus, which match the internal data paths. The memory bus is pipelined, allowing an operation to start while other operations are finishing. The 2-level pipeline lets up to 3 memory operations execute at one time. The i860 supports both big- and little-endian addressing.

Cache coherency—The original XR had a copyback cache scheme, which made implementing i860 multiprocessor configurations difficult. The XP implements the MESI (modified, exclusive, shared, invalid) cache-coherency protocol for multiprocessing. Additionally, the XP handles 1-cycle burst writes. The XP implements both write-through and write-back caching. Another processor can check to see if an address is in an i860's caches.

Pipeline recovery—The i860 has an exposed, programmable FPU pipeline. An interrupt can require saving a pipeline's status and data. The i860XP has a quick fix to minimize overhead: If ISRs don't use the pipeline, they don't have to save and restore it. To ensure that the pipeline is not disturbed, ISRs can set a status bit, which triggers an exception if the pipeline is touched.

i860XP

Current (max)	Voltage (V)	Clock (MHz)
1.2A	5	50

In 262-pin PGA.

Intel's i860 has a classic RISC architecture. The processor is built around a 4-stage pipeline, has a simple load/store instruction set, and uses a fixed-length, aligned 32-bit instruction word. The i860 has a set of 32 32-bit general-purpose registers and 6 control registers including a PSW, extended PSW, data-breakpoint register, and directory base register. The on-chip floating-point unit (FPU) has its own eight 128-bit floating-point registers, which are also addressable as 16 64-bit registers.

But the i860 is more than just a RISC processor: It can start two instructions—one CPU and one FPU—in a single clock cycle. The i860 has a total of four execution units: the core RISC processor, the floating-point multiplier, the floating-point adder, and the graphics processor. Dual instructions can also be issued for a floating-point unit and the graphics processor unit. In fact, the i860 is really a VLIW—a very-large-instruction-word—processor because it can take in two instructions at a time (64 bits) and issue each to a processing unit.

The core RISC processor has a small, simple instruction set with standard 3-address instructions. Instructions and data are cached to increase execution rates. The original i860 had a 4-kbyte instruction cache and an 8-byte data cache. The latest XP version hiked cache sizes to 16 kbytes each. The caches are 4-way set associative and have a 32-byte line size. Data and instruction paths to the decoder or CPU register file are 128 bits wide. The wide data paths let the CPU move 128 bits (4 words) at a time between the data cache and the register files for high-speed throughput.

FPU processing meets ANSI/IEEE 754 standards. Both the adder and multiplier units are pipelined; the adder has three stages, the multiplier has four. The floating-point adder and multiplier can run concurrently, performing a multiply-accumulate cycle suitable for vector and matrix processing. The FPU has two pipeline execution modes. In one, the next instruction is fetched and decoded, but execution is held up until the execution unit is free. In the other mode, instructions start in the execution unit at each clock (every other clock in the multiplier unit for double precision). There is no floating-point divide. The FPU does divides and square roots using the Newton-Rhapson software algorithms. Also there is no integer multiplier. Hardware uses the floating-point multiplier.

The on-chip 3-D graphics unit is an execution unit in parallel with the floating-point adder and multiplier. The 128-bit floating-point register file feeds the graphics unit, which handles 8- to 32-bit pixels and can process 128 bits worth of pixels each cycle. Z-buffer check instructions compare the Z-buffer values (pixel depth), selecting the nearest pixel for eliminating hidden lines in wireframe and 3-D displays. Instructions load and store pixels and interpolate intensities for the pixels along display surfaces. Pixels are loaded, interpolated, and manipulated in 128-bit chunks.

Graphics instructions—Pixel store, Z-buffer check, add with pixel/Z merge, OR with pixel merge. Operations on 4-, 8-, 16-, 32-, or 64-bit pixels are combined in 64-bit words. Many operations are pipelined.

Floating-point instructions—Autoincrement addressing mode for loads/stores (adds item displacement to addr). Floating-point instr control each stage of floating-point adder and multiplier, can coordinate concurrent multiply-accumulate operations. Sources and destinations can be specified for each pipeline stage operation. Special reg can hold a multiplier constant, freeing up an adder input line.

Special instructions—Floating-point/integer compare, branch loop and add (increments loop counter), lock/unlock, indirect subroutine call. Bit operations are at the word logic level.

SUPPORT

□ HARDWARE

The i860 implements a hardware data-breakpoint register. A virtual-address access to an address held in this register will trigger a trap. Masking off a number of low-order bits lets the data-breakpoint register specify a block of memory. Logic analyzers are available from several vendors for the i860. The family has no ICEs.

□ SOFTWARE

Intel's development tools for the i860 include an assembler/linker, C compiler, Fortran compiler, and instruction-set simulator and debugger, and math and graphics libraries. Third-party vendors provide C, Fortran, and Ada compilers. Unix System Labs (Morristown, NJ) supplies a native Unix binary and a source copy for OEM customization.

□ **OVERVIEW** Intel's 32-bit i960 RISC μCs target both military and commercial embedded applications. First introduced in 1989, the family ranges from low-end SAs with 16-bit external buses to superscalar CAs and CFs to military-specific processors such as the MX, which has dual external buses and built-in security and multiprocessing features. The family has penetrated the embedded-systems world in applications such as laser printers, graphics processing, telecommunications, and data staging. Superscalar i960s achieve 2 to 3 sustained instruction executions per clock cycle. In fact, the i960 has been selected by the Joint Integrated Avionics Working Group (JIAWG) as a 32-bit standard CPU for military flight-control avionics.

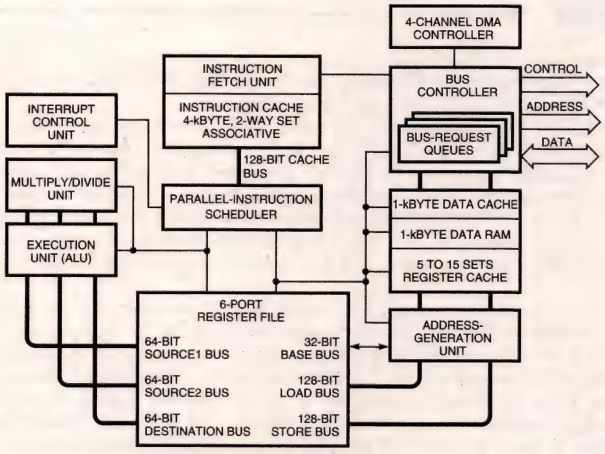
□ **VENDORS/PRICING** Intel is the developer and sole supplier.

16-MHz i960SA, $22.95; 25-MHz i960KA, $51.10; 25-MHz i960MC, $516; 33-MHz i960CA, $121.05; 33-MHz i960CF, $181.60 (1000).

Intel i960

- 32-bit reg-based RISC processors
- 32 regs: 16 local, 16 global
- Reg cache holds 4 to 15 sets of local regs
- 512 bytes to 4 kbytes instr cache
- Superscalar processing, 4-instr decoder (CA/CF/MM)
- Unified addr space
- 32-bit ext bus, burst mode
- Store buffering, load bypass
- Advanced memory: I/O interface with DMA, I/O control (CA)
- 4 to 9 ext intr
- Military versions have MMU
- 20- to 66-MHz clock (divide-by-2 internal)
- 128/256-bit internal buses move instr, data
- Superscalar operation (CA/CF/MM): issue up to 3 instr/clock, sustain 2
- 1-clock ADD (pipelined)
- 5-clock MPY, 36-clock DIV (33-MHz CF).
- 750-nsec context switch with reg cache (33-MHz CA)
- 59-Mbyte/sec DMA rate (33-MHz CA)
- Interruptible long instr
- 1-μsec intr latency (33-MHz CF)

ARCHITECTURE



Intel's i960 is a hard architecture to classify. i960s combine a von Neumann architecture, RISC implementation techniques, CISC instructions, complex addressing modes, 184 instructions, microcode, a register file, register-window caching, a sophisticated I/O controller, a complex interrupt controller, and superscalar (more than one instruction per cycle) operation. Military-specific parts have MMUs and special control capabilities. i960s run the gamut from a bare-bones, minimal RISC chip to a complex, multiple, external bus, superscalar military μC.

Operations center on a core of 32 32-bit general-purpose registers divided into 16 local and 16 global registers. An on-chip register cache caches the local register sets, holding 4 to 15 sets. Register caching speeds context switching because hardware automatically caches register sets. If the cache is full, the oldest cached set is moved to memory and the latest set cached.

The 960SA/SB/KA/KB low-end chips have small Register and instruction caches. They implement a set of 173 instructions, have a 5-stage pipeline, and use register scoreboarding to track resource usage and which instructions can execute. The CPUs allow out-of-order execution—a later instruction can execute while a prior one waits for a critical resource to become free.

The i960CA moved up to superscalar operation. The key to the CA is its 4-instruction-wide instruction decoder, which decodes up to 4 instructions per cycle. Current implementations dispatch up to 3 of these instructions for execution. Wide internal buses move instructions and data between execution units. The i960CF has 256-bit-wide buses to move instructions to the decoder and 128-bit-wide buses to move data between the cache and registers. There are three pipeline stages: fetch, decode, and execute.

Superscalar i960s are built around a 6-ported register file, with execution units gathered into 2 groups, register control and memory control. These units include floating-point integer, floating-point MPY/DIV, integer MPY/DIV, integer, and interrupt control units on the register side; and address-generation, MMU, and bus-controller units on the memory side. Instructions are cached in a lockable cache, later versions added an instruction cache to supplement the register cache.

Military i960s include an MMU for protection and virtual addressing. Superscalar MX and MM versions opened up the CA's 32-bit multiplexed/nonmultiplexed bus. The controllers implemented two buses: a slow 32-bit multiplexed system bus (1/2 system clock) for I/O and a 64-bit "backside" bus for local-memory access (23-bit addr, up to 1 Mbyte).

I/O controller—CA and later versions have 4-channel DMA controller that also functions as a classic I/O controller to optimize I/O. Controller handles data chaining (gather/scatter), data packing, and unpacking.

Multitasking/multiprocessing—Military and first-generation i960s have hardware multitasking/multiprocessing capabilities. Interagent communications defines messaging system for multiple CPUs. MX CPU queues tasks for execution; communications ports asynchronously exchange parameters between CPUs. Atomic instructions synchronize CPUs.

□ **VARIATIONS**

i960KA/KB/MC—First i960s. 16/20/25 MHz, 512 bytes instr cache, 64×32-bit reg cache, 32-bit multiplexed ext bus, 4-word burst, 4 ext intr, 132-pin PGA/QFP. MC is mil-temp-range version.

i960SA/SB—Stripped-down KA/KB. 10/16 MHz, 512 bytes instr cache, 64×32-bit reg cache, multiplexed ext bus (32-bit addr, 16-bit data), 4-word burst, 4 ext intr. SB adds FPU.

i960CA/CF—Superscalar i960. 16/25/33 MHz, up to 4 kbytes instr cache, 1 kbyte data RAM, 1 kbyte data cache, reg cache (up to 15 sets in data RAM), 4 DMA channels, DMA controller with data chaining, packing, and unpacking. 32-bit nonmultiplexed external bus has dynamic sizing, intr controller (248 possible intr). 16 separately configurable physical-memory regions. 168/196-pin PGA/QFP.

i960MM—Expanded CA for military. Superscalar; has FPU and MMU. 25 MHz, 2 kbytes instr cache, 2 kbytes data cache, 2 ext buses (32-bit system bus, 64-bit backside bus), mil temp range. Available on evaluation board.

i960MX—Expanded CA for military. Superscalar, 25 MHz, 2 kbytes instr cache, 2 kbytes data cache, 512 bytes reg cache (8 local sets), FPU, MMU, 2 integer units, 33rd tag bit (differentiates object, pointer), two ext buses (32-bit system bus, 64-bit backside bus), JIAWG compatible, multitasking capability, mil temp range, 348-pin PGA.

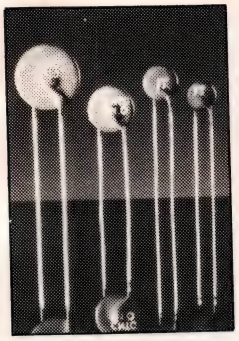
Version	Current (max)	Voltage (V)	Clock (MHz)
SA/SB	350 μA	5	16
KA/KB/MC	480 mA	5	25
CA	900 mA	5	33

CA in 168/192-pin PGA/QFP; SA in 84/80-pin QFP/PLCC.

SUPPORT

□ **HARDWARE** The i960 has built-in debugging features. The chips have 2 to 4 hardware breakpoint registers and 2 instructions for setting software breakpoints. ICEs and logic analyzers are available for the processors. Intel provides evaluation boards for most i960s.

□ **SOFTWARE** The i960 enjoys a full range of development and operating software including real-time kernels and operating systems. Compilers include C, Ada, and Fortran. Intel has developed a C compiler that builds a profile of each program and task and then optimizes the code based on the code's operational characteristics.



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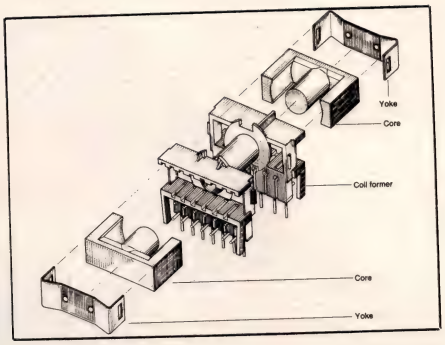

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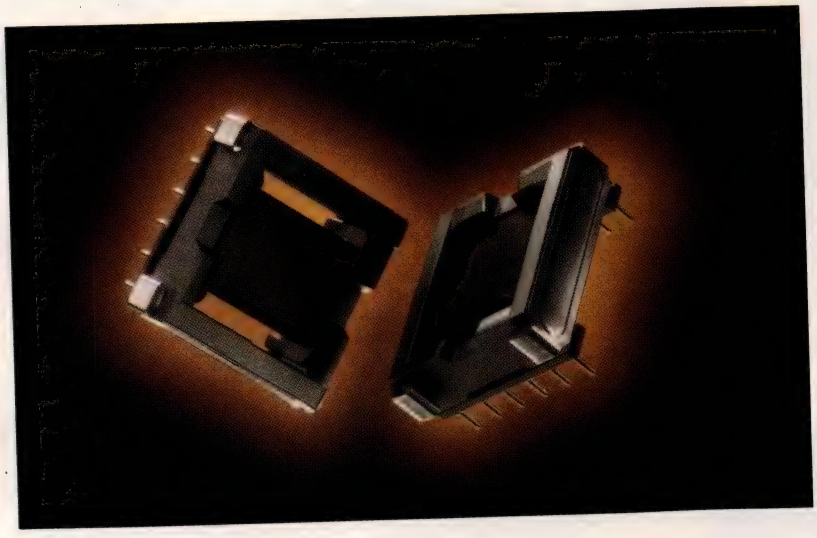

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CIRCLE NO. 58

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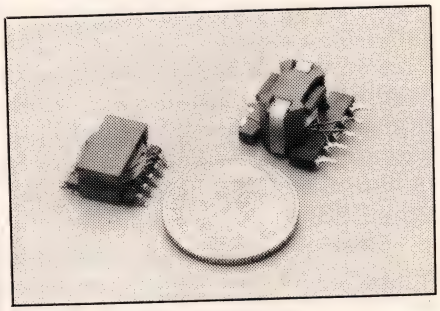

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CIRCLE NO. 63

Mips R3000

- 32-bit RISC μP, 32 32-bit regs
- 115,000 transistors (R3000)
- 74 instr
- 5-stage pipeline
- On-chip FPU or off-chip FPU coprocessor
- Dual ext caches, on-chip cache control
- 2 to 16 kbytes on-chip instr and data caches (embedded versions)
- 64-entry TLB, MMU
- 32-bit ext addr, data buses
- Multiplexed ext bus (embedded versions)
- 16- to 40-MHz ext clock
- 1-cycle instr execution (pipelined)
- 12-cycle MPY
- 35-cycle DIV (software)
- Dual ext caches accessed at 2×clock rate
- 1-cycle branch delay
- 1-cycle mem R/W (load-delay slot)
- 2-cycle load/use penalty
- 35-cycle intr latency

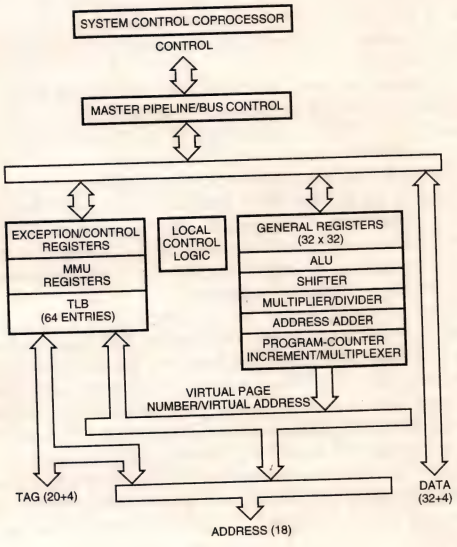
□ **OVERVIEW** Developed initially at Stanford University, the 32-bit Mips RISC architecture was one of the first commercial RISC microprocessors. A classic RISC design, Mips μPs were the speed demons of first-generation RISC processors but burdened system designers with a complex off-chip dual-caching scheme. The μPs are known for their sophisticated design and the advanced code optimization their compilers achieve. Licensed chip vendors have used the Mips core and architecture as a base for embedded processors, many adding on-chip caches and reducing pinouts. R2000/3000 Mips CPUs generally use an off-chip FPU; some R3000 versions have an on-chip FPU.

□ **VENDORS/PRICING** Mips Technologies Inc, now part of Silicon Graphics, develops Mips chips and licenses them for manufacturing. Licensed vendors include IDT, LSI Logic, NEC, Performance Semiconductor, and Siemens. Some vendors have architectural licenses, which lets them modify chip designs.

LR3300 (25/40 MHz), $69/$134; L33020 (25/40 MHz), $99/$167; LR33050, (25/40 MHz), $122/$333; Piper (40 MHz), $600; PR3400 (40 MHz), $203; LR3400AN, (40 MHz), $76.

Integrated Device Technology: IDT79R3001 (20 MHz), $68; IDT79R3041 (16 MHz), $15 (50,000); IDT79R3051 (20/40 MHz), $29/$70 (1000); IDT79R3052 (20/40 MHz), $43/$98 (1000).

ARCHITECTURE



The Mips architecture was the speed demon of the first-generation 32-bit RISC processor pack. A classic RISC design, Mips RISC chips use tight chip and system design to minimize silicon and deliver computing performance. The architecture reflects a strict adherence to chip design and layout constraints. Mips also developed an effective compiler technology for optimizing RISC code. Much of the early Mips architecture and software research was done at Stanford University, some under government research grants.

Mips processors are built around a set of 32-bit general-purpose registers in a central register file. To minimize control logic, the instruction set is reduced to 73 instructions, addressing options are limited, and the chip has a 3-address, load/store architecture. Similarly, instruction sizes are fixed to one 32-bit word to minimize decoding and speed processing.

Like many early RISC μPs, Mips CPUs balanced throughput against complex instructions, including multiply and divide. The R2000 had limited multiply and divide capabilities. Later Mips CPUs added a full multiply but have limited divide capability. The CPUs have provisions for multiple coprocessors. Initially, Mips chips used an external FPU, but later R3000 versions have brought the FPU on chip.

Mips engineers used a 5-stage pipeline for the R2000 and R3000. The pipeline lets up to 5 instructions execute concurrently—each at a different stage of its instruction cycle—thus giving the effect of single-cycle execution. The pipeline stages are instruction fetch (IF), read operands and decode instruction (RD), execute (ALU), access data memory (MEM), and write-back results (WB). A branch-delay slot minimizes branch effects. The compiler fills the instruction slot following the branch with an NOP or an instruction from the current thread that can be executed before the branch takes effect.

The Mips R2000 and R3000 rely on off-chip caches. The μPs have the cache-control logic and a MMU/TLB to access the caches. For high performance, Mips engineers devised a dual-cache scheme: 2 caches hang off the main bus and the CPU can access both during a single clock cycle. Thus, each cache is accessed at twice the system clock rate. This cache scheme sets fundamental performance limits for the R2000/R3000 architecture. Clock rates faster than 30 to 40 MHz require cache accesses at 60 to 80 MHz, which pushes the limits of board and chip design. The new R4000 avoids this problem by adding 2 on-chip, 8-kbyte caches and a redesigned memory interface. Many Mips chip vendors took a similar approach for embedded R2000/R3000 chips by adding on-chip cache or running the processor with a single external cache.

Chip	Current (max at 5V)	Package
LR33000	600 mA	155-pin PGA
LR33050	900 mA	160-pin QFP
Piper (3.3V)	1.3A(500 mA)	160-pin QFP
R3051	900 mA	84-pin PGA

VARIATIONS

R3000A—Up to 40 MHz, off-chip caches, on-chip cache control, 144-pin PGA, 160/172-pin QFP.

IDT79R3041—Embedded R3000, 16/20 MHz, variable bus sizing, 2-kbyte instr cache, 512-byte data cache, 84-pin PLCC.

IDT79R3051/52—Embedded R3000, 20 to 40 MHz, 6-kbyte instr cache, 10-kbyte data cache, 4-deep R/W buffer to memory, multiplexed ext bus, 84-pin PLCC.

LSI Logic CoreWare (CW33000)—R3000 core for ASICs. Library includes basic CPU core, core with 2/4-kbyte instr cache, 1-kbyte data cache.

LR3300—Embedded R3000, 25/30/40 MHz, static design, 8-kbyte instr cache, 1-kbyte data cache, 3 counter/timers, DRAM controller, nonmultiplexed bus, 155-pin QFP.

LR33020—Embedded R3000 for X-terminals; re-implemented core; static design; 4-kbyte instr cache; 1-kbyte data cache; graphics coprocessor with bitblt processor and DMA channel; 224-pin PGA; 208-pin QFP.

LR33050—Embedded R3000, on-chip FPU, 4-kbyte instr cache, 1-kbyte data cache, timer/counters, DRAM controller, 4-word write buffer, burst mode, nonmultiplexed ext bus, 155-pin PGA, 160-pin QFP.

Piper—Embedded R3000A, on-chip FPU, 35/40/45 MHz, 8/4-kbyte instr cache, 2/4-kbyte data cache, on-chip FPU, 4-deep write buffer, multiplexed ext bus, 6 ext intr, 3.3 or 5V, 160-pin QFP.

PIMM—R3000A multichip module in PGA package. On-chip FPU, 32-kbyte instr and data caches, 25/33/37/40 MHz, 144-pin PGA.

SUPPORT

□ **HARDWARE** The Mips design is a straightforward, minimal architecture with bare-bones test features. Hardware tools include ICEs or logic analyzers for most Mips chips. Additionally, most chip vendors sell evaluation boards for development and test.

□ **SOFTWARE** Mips provides native- and cross-development tools, which are also furnished by chip vendors. Tools include a system simulator, cache-design and -optimization tools, and host/target debugger software. Mips compilers effectively optimize code execution on the RISC CPUs. Unix and real-time kernels are available for Mips processors. Application software includes page-description languages, X-servers, and PROM monitors.

□ **OVERVIEW** Motorola's 68K μPs were early leaders in mid- to high-end μP applications. In the late 80s, the 68K lost workstations and servers to RISC processors, but the 32-bit 680x0 family is now firmly rooted in mid- to high-end embedded monitor/control systems. They power upper-end Macintoshes and the Next workstation and are the leading CISC processor for printers. The 680x0 architecture is built around 16 general registers and a usable, orthogonal instruction set and has a wide range of hardware and software development tools. Heading the 680x0 lineup is the 68040, which combines RISC and CISC technologies and has dual 4-kbyte caches, an FPU, and an MMU. Still in the game are the 68020 and 68030—CISC implementations with smaller caches. Motorola has introduced stripped-down 68EC0x0 versions and the 68LC040, both of which have a simpler external bus and no FPU.

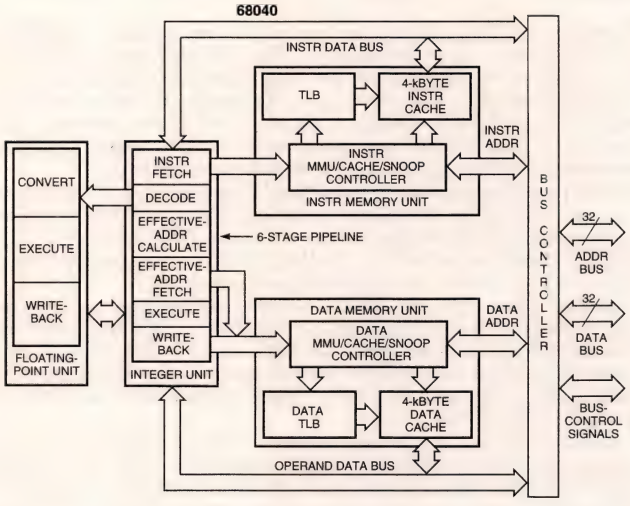
□ **VENDORS/PRICING** Motorola developed the 680x0 family and is the sole source.

68020/30/40 (16/16/25 MHz, QFP), $26.30/$64/$337; 68EC20/30/40 (16/25/20 MHz, QFP), $15.10/$36.85/$94.75.

Motorola 680x0

- 32-bit μP family; 68000, 68302/6, 16 bits
- 98 instr (040 has 144), superset of 68000 CISC instr set
- 8 data, 7 addr regs; 11 floating-point regs (040)
- 2 4-kbyte instr, data caches (040)
- 128-byte instr cache (020); 2 256-byte caches (030); 2 4-kbyte caches (040)
- 32-bit ext addr, data buses; nonmultiplexed
- 25/33/40 MHz (040); 20/25/33/40/50 MHz (030)
- 22/36 native MIPS sustained (040 at 25/40 MHz)
- 2-clock ADD, NOP (030)
- 1-clock ADD, NOP (040)
- 5-clock mem-reg ADD (040)
- 17-clock MPY, 35-clock DIV (040)
- 2-clock ext mem R/W, 1 clock in burst (040)
- 70-clock intr latency; 7 intr levels, 255 types (EC040/40)

ARCHITECTURE



The 680x0 family is the 32-bit extension of the 16-bit 68000 μP. The original 68000 instruction set and register organization is the core of the 680x0 family. The 680x0 has sixteen 32-bit general-purpose registers (8 data, 7 address, 1 SP) coupled with a highly structured, orthogonal instruction set. The family handles multiple-register moves, bit and stack processing, and 18 addressing modes.

The processing features the 68020/30/40 added to the 68000 include floating-point processing, memory management, dynamic bus sizing, and on-chip caches. The 68020 and the 68030 rely on FPU coprocessors (68881, 68882); the 68040 integrates an FPU on chip.

The 680x0 has more registers than the original 68000—control registers were added to control the MMU and the FPU, as well as support additional processing capabilities. For example, the 68040 adds eight 80-bit floating-point registers and 12 control registers. These include a vector-base register (points to interrupt vector table), cache-control register, user and supervisor root pointers, and translation registers.

The 680x0 is basically a CISC architecture; many instructions are complex, and the ALU operates on both register and memory data. The 68040 also has RISC-like implementation features. For one thing, it has a 6-stage pipeline (fetch, decode, effective-address calculate, effective-address fetch, execute, and write back). To speed processing, it has two on-chip 4-kbyte direct-mapped caches, and separate data and instruction MMUs, which allow simultaneous address translations. Bus snooping is built into the 040's caches to ensure cache coherency for multiprocessing. Both write-through and copy-back modes are built into the cache. Both the 030 and 040 implement burst mode, moving up to 16 bytes in a single addressing block between registers and memory.

The 040 delivers apparent single-cycle execution for some instructions, mainly register operations such as memory-to-register moves (if the data is in the data cache). A taken branch takes 2 cycles; a not-taken branch takes 3. Unlike the 020/030, the 040 does not do dynamic bus sizing. Instead, it has a highly reliable bus with a high-drive option and implements a synchronous, 2-clock R/W protocol. A 4-word burst takes 5 clocks. Multiprocessor bus arbitration is built into the 040 but requires off-chip logic.

Additional instructions—Instr for variable-length bit fields, moving 16 regs, compare and swap (locks memory for multiprocessing). Scaling option for addressing—scales addr by item size for table-access, FPU, MMU commands.

Caches—The 020's instr cache is 128 bytes. The 030 has two 256-byte instr and data caches; the 68040 has two 4-kbyte caches.

□ VARIATIONS

68040—Top of the line; has some RISC features. Small output buffer and high drive impedance. Independent MMUs for instr and data. Multimaster/multiprocessor support with bus snooping for cache coherency. Selectable output impedance. 25/40 MHz.

68030—On-chip MMU; 2 256-byte caches (instr and data); nonmultiplexed, 32-bit data and addr bus; burst mode (to 16 bytes). 20, 25, 33, 40, 50 MHz.

68020—First 32-bit version of 68000. Expanded instruction set; coprocessor interface for FPU (68881, 68882); 128-byte instr cache; on-chip MMU. 12, 16, 20, 25, 33 MHz. 100-pin QFP, PGA.

EC versions—Cut down, CMOS versions of the 680x0. 68EC020: 24-bit addr bus (to 24 Mbytes), dynamic data-bus sizing (8 to 32 bits), 256-byte instr cache. 68EC030: 25/40-MHz clock, burst-mode, dynamic bus sizing, PGA. 68EC040: No FPU, MMU, high output-drive option, or multiplexed ext bus modes. Two 4-kbyte caches; 179-lead PGA.

μP	Current (max)	Voltage (V)	Clock (MHz)
68EC020	320 mA	5	25
68EC030	370 mA	5	40
68EC040	1.26A	5	33

020 in 100-pin PGA, QFP; 030 in 124/132-pin PGA, QFP; 040 in 179-pin PGA.

SUPPORT

□ **HARDWARE** The 68000 family, including the 680x0 μPs, has built up a large hardware-development-tool base including ICEs and logic analyzers. Evaluation boards are available from Motorola as well as third parties. 680x0 workstation/servers are also available for cross development. 680x0 boards are a standard VMEbus platform and are used as both target and host-development systems.

□ **SOFTWARE** The 680x0 family has a plethora of operating and development software. Unix and other operating systems as well as real-time kernels run on 680x0s. PC, workstation, and native development systems, compilers, and simulators are available. Compilers include C, C++, Fortran, Ada, Forth, Pascal, Modula-2, Basic, Cobol, Lisp, PL/I, Prolog, and RPG. Native- and cross-development assemblers and linkers are also available.

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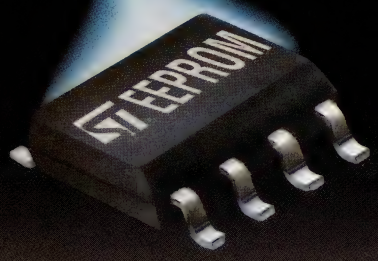

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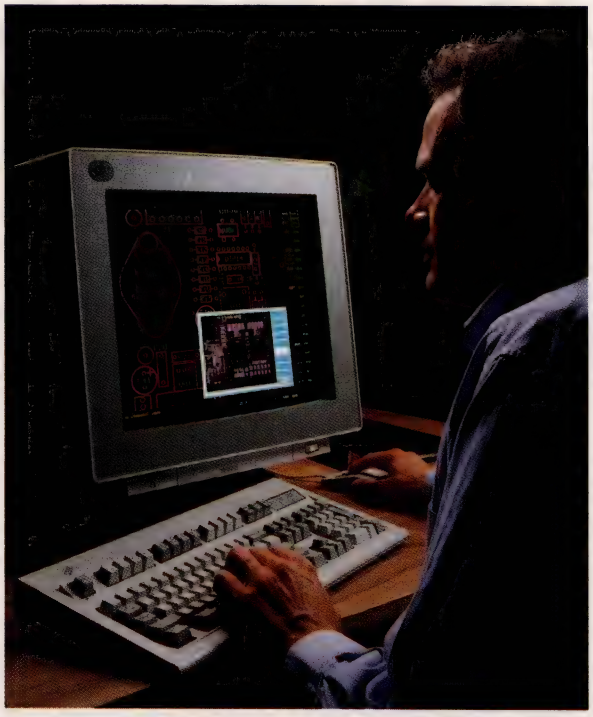

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Motorola 683xx

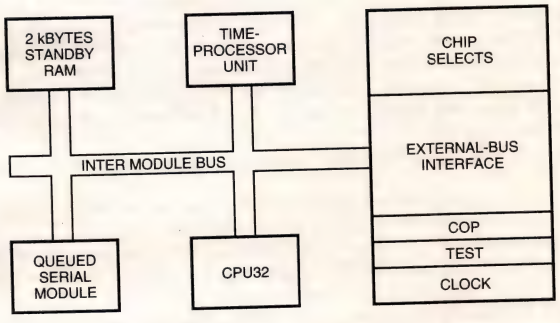
- Complex processor with reduced 68020 core
- 87 instr, 68020 instr subset
- 8 general data, 8 addr regs
- No ROM; 2 kbytes RAM (332)
- 48 kbytes flash EEPROM; 4 kbytes RAM (333)
- Ext bus: 24- to 32-bit addr, 8- or 16-bit data (dynamic sizing)
- 8/12 chip selects, 16 I/Os, 7 ext intr
- Inter Module bus with DMA
- 16.78/25.1-MHz internal clock (8.39 MHz at 3.3V) from 32-kHz/4-MHz ext clock with PLL
- 120-nsec NOP, ADD
- 3.10-μsec 32-bit MPY; 2.74-μsec DIV
- 2-clock memory access
- 50-Mbyte/sec burst DMA transfer rate (25.1 MHz)
- PWM: 24-bit resolution, 80-nsec at 25.1 MHz (68340)
- 590-cycle max intr latency (68332)

□ **OVERVIEW** The 683xx family represents a new direction in embedded μPs: Using a well-known μP core as a base and adding advanced peripherals that offload the CPU. Rather than create a new 32-bit μP, Motorola integrated a stripped-down 68020 core with an Inter Module bus and complex peripherals. These peripherals include a time processor unit, which offloads timer/counter functions and has its own controller, and a queued serial module, a serial communications controller that queues data for polling and event processing. Two versions, the 68302 and 68306, use the 16-bit 68000 CPU as the core (see 68000 entry). One chip, the 68F333, has 48 kbytes of flash EEPROM.

□ **VENDORS/PRICING** Motorola developed the 683xx family and is the sole source.

68330 (4 chip selects, 132-pin QFP), $17.10; 68332 (1152 bytes SRAM, queued serial module, time processor unit, ADC, 132-pin QFP), $20.54; 68331 (queued serial module, general-purpose timer, 132-pin QFP), $16.18; 68340 (2-channel DMA memory controller, 2-channel serial I/O, 2 timer modules, 144-pin QFP), $23.40.

ARCHITECTURE



Two generations of engineers cut their design teeth on Motorola 68000/680x0 μPs. The 683xxx family builds on that processor base. The core is a stripped-down, 32-bit 68020. It links to a 16-bit on-chip Inter Module bus, which provides a data highway between the CPU and chip peripherals and makes adding or swapping peripherals easy.

The core processor, the CPU32, is the 68020 CPU modified for embedded control—no MMU or FPU interface. The 32-bit processor has 8 general 32-bit registers; seven 32-bit address registers; a 32-bit ALU; separate user and supervisor modes, each with its own SP and address space; and separate address and data spaces. The CPU32 is code compatible with the 68020 but has enhanced addressing modes including scaled index, address register indirect with base displacement and index, PC relative, and 32-bit branch displacements. Post- and pre-increment/decrement options simplify iterative code. Peripheral-control registers and I/O are memory mapped; the CPU accesses them as addresses in memory.

The 683xx is not easy to classify as a μP or μC. The 68332 μP with 2 kbytes of on-chip RAM needs external memory, but the 68F333 has 48 kbytes of flash memory and 4 kbytes of RAM, making it a μC. The 68340 has no on-chip memory. Most 683xx chips run from external memory, which classifies them as μPs rather than μCs. The memory interfaces are 8 or 16 bits wide for data and from 24 to 32 bits wide for external addressing lines. Data bus size is dynamically sizable.

The 683xxx represents a new direction in embedded control: integrating existing CPUs with mixtures of peripherals, some extremely complex. The peripherals handle classic peripheral functions, and many also offload the CPU by doing their own processing.

The time processor unit includes its own processor and runs independently from the CPU32. The unit lets you program control and timing functions that don't use CPU resources. These functions include PWM, stepper-motor control, input capture and output compare, pulse accumulation, frequency measurement, and timer functions. The CPU passes data to the time processor unit via dual-ported SRAM. Simpler timer peripherals are also available in the 683xx family, including a general-purpose timer set, timer array, and sets of standard timer/counters.

68020 instructions not supported—BCD pack/unpack, bit field, compare and swap, coprocessor, MMU, module call/return. Memory indirect addressing also not supported.

New instructions—Table look-up and interpolate; put chip into low-power, standby mode; put chip into background mode for test.

Background mode—Allows host control of 683xx via test port. Using the test port an ext device can fill or dump memory, patch user code (direct execution to code patch), and read or write memory or regs. Builds some ICE-like features into the hardware.

□ PERIPHERALS/VARIATIONS

Queued serial module—Provides 2 interfaces: queued serial peripheral interface (a full-duplex synchronous line) and serial communications interface (a full-duplex UART). Queued peripheral interface queues and processes data. Module can repeat cycles, providing polling and loop processing. 80 bytes SRAM for local storage of receive, transmit, and control data.

System-integration module—Ext memory interface with 24 addr, 16 data, and up to 12 programmable chip-select lines. Includes watchdog and periodic timers, and clock-generation circuit with PLL to boost 32-kHz/4-MHz ext clock to 16.78- or 25.1-MHz internal clock.

Time processor unit—Handles 16 timer channels; has its own microengine with ROM control store. The host interface holds parameter in dual-ported RAM regs for processing. Each channel is fully independent and has its own I/O pin, 16-bit compare-and-capture regs, and comparator. Time kept by 2 free-running counter regs shared by the channels. Minimum time resolution is 500 nsec.

General-purpose timer—Simpler timer/counter. Includes compare/capture unit with 1-channel, 16-bit timer; 8-bit pulse accumulator, 9-stage clock prescaler, PWM unit (16-bit free-running counter with 2 channels). Stop mode.

68330

Mode	Current (max)	Voltage (V)	Clock (MHz)
Run	120 mA	5.0	16.78
Low power	300 μA	5.0	16.78

In 132-pin static QFP.

SUPPORT

□ **HARDWARE** The 683xx family's background mode gives the chips a built-in test capability. In background mode, tools can control the processor and read and set register and memory values. Users can also patch in code and have the processor execute a code patch in another location for a given PC value. Some ICEs and logic emulators are available, and Motorola has evaluation boards for the chips.

□ **SOFTWARE** Development software includes cross-assemblers/linkers, C and Modula-2 compilers, and a simulator and software branch analyzer. Operating software includes at least four real-time kernels, including one full operating system, and an integrated host/target development environment.

Motorola 88000

- Specs for 88110: 32 32-bit CPU regs, 32 80-bit floating-point regs
- 1.3M transistors
- 66 instr (51 for 88100)
- 4-stage pipeline
- Superscalar operation
- 10 functional units: 2 graphics, MPY, DIV, floating-point ADD, load/store, 2 integer, bit field, instr/branch
- Branch prediction, target-instr cache
- 8-kbyte instr, data caches
- 64-bit pipelined ext bus; burst, split modes
- 6 80-bit internal buses
- Specs for 88110: 40, 50 MHz (88100, 16 to 33 MHz)
- Issues up to 2 instr/clock
- 64 SPEC89marks, 75 with ext cache (estimated)
- 1-clock execution (pipelined)
- 3-clock mem-reg ADD
- 3-clock MPY; 13-clock DIV
- 2-clock ext-bus R/W
- 1-clock burst-mode R/W (plus 1)
- Branch-delay slot
- Out-of-order execution
- Target-instr cache, no penalty for correct branch
- Branch-prediction bit, 1-clock penalty if wrong

□ OVERVIEW

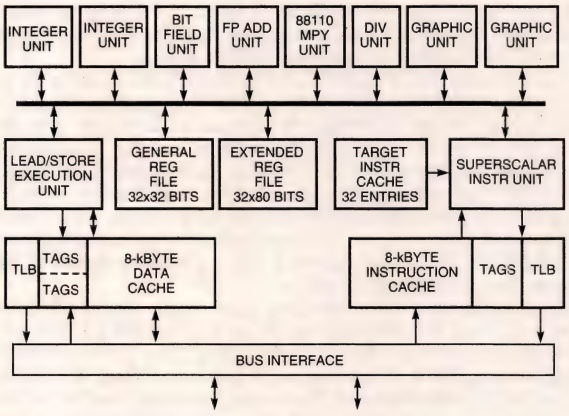
Introduced in 1988, Motorola's 88000 RISC family arrived too late to become a major player in the RISC/Unix workstation/server world. Yet Motorola and other systems houses use the μP family, and prices have come down dramatically. The first family member, the 88100, has an enhanced first-generation RISC architecture. Features include an on-chip FPU, scoreboarded registers, simple instructions and addressing modes, and a load-store architecture. The CPU has a Harvard architecture with dual instruction- and data-cache buses and uses special cache/MMU chips for off-chip memory. The 88110 introduced in 1992 is a sophisticated second-generation RISC μP. The superscalar chip issues up to two instructions per clock cycle. The 88110 has two 8-kbyte on-chip caches, an improved cache/memory bus, and 8 superscalar functional units, including two specialized units for graphics pixel processing. The 88110 can run directly from DRAM or a secondary cache. The 88410 cache controller handles up to 1 Mbyte of fast SRAM.

□ VENDORS/PRICING

Motorola is the developer and sole source of the 88000 family.

88110 (50 MHz), sample pricing $495 (1); 88100 (16 MHz), $49 (33 MHz, $130); 88200 cache/MMU (16 MHz), $75 (33 MHz, $188).

ARCHITECTURE



□ VARIATIONS

88110—Superscalar 88000, can issue 2 instructions per clock cycle. 1.3M transistors, 64-bit nonmultiplexed bus. Handles 4 double-word bursts, split (pipelined) transactions. Has separate 80-bit FPU reg file and on-chip 8-kbyte cache and MMU for data and another set for code. Upward compatible with 88100. 10 functional execution units including graphics and FPU. Ext bus interfaces to cache controller or DRAM, supports bursts for page-mode or static-column DRAM. Split-transaction bus lets another CPU start cycle while current one completes.

88410—Secondary-cache controller, can handle 0.25, 0.5, or 1 Mbyte of secondary cache using 15- to 20-nsec SRAMs. Provides bus arbitration and can handle multiprocessing. Accesses take 1 wait state on initial access, 0 wait states on subsequent burst accesses. Chip requires no glue logic. Up to two 88410s can be used at full speed with up to 2 Mbytes of cache. Half-speed-bus option for slower systems.

88000—First-generation 88000. On-chip FPU shares single register file. Scoreboarded registers. No on-chip cache, MMU. Has separate data- and instr-cache ext buses. Uses 88204 cache/MMU chips for high-speed caching.

88100/88110

Chip	Current (max at 5V)	Clock (MHz)
88110	2A	50
88410	600 mA	50
88100	300 mA	33
88204	200 mA	33

88110 in 299-pin PGA;
88100 in 180-pin PGA.

The 88000 ISA architecture was designed as a base for multiple implementations. The initial 88100 combined RISC features—such as a load/store architecture, simple instruction set and addressing modes, and a block of general registers—with register scoreboarding, an on-chip FPU that shares the general registers, and a Harvard architecture with separate buses for data and instruction memory. The 88100 has no on-chip cache. Instead, it uses external data and instruction caches. The 88100 also uses chips that integrate the MMU with SRAM cache. The latest such chip, the 88204, holds 64 kbytes of memory. Multiple 88204s can be used in parallel to increase cache size.

The 88110, an advanced superscalar μP, eliminates many of the bottlenecks of the earlier 88100. The 88110 adds two 8-kbyte, 2-way set-associative caches and has a separate floating-point register set—32, 80-bit registers—to relieve the FPU-CPU register-set bottleneck. (Both integer and floating-point operations use the same register set in the 88100.)

88110 operations center on the register files and two sets of 80-bit-wide execution buses. Each register file handles 4 reads and 2 writes per clock cycle so the CPU can execute 2 instructions per cycle. The bus sets—each has 2 source buses and 1 destination bus—hook up 10 functional units. Up to 2 function units get execution orders each clock cycle. Functional units include 2 integer, 1 bit manipulation, 1 multiply, 1 divide, 1 floating-point adder, 2 graphics pixel-processing units, 1 load/store, and 1 instr/branch.

The 88110 has a 4-stage pipeline. It can issue a maximum of two instructions per clock cycle. Two ADDs can execute in parallel as long as one doesn't require the data produced by the other. Register scoreboarding tracks register dependencies and stalls instructions that use registers currently in play.

The 88110 issues instructions in program order but performs out-of-order execution and completion. The CPU does speculative execution: It will start an execution instruction thread before the branch direction is certain by using branch prediction. If it predicts the wrong branch, the CPU backs up using a 12-entry history buffer and begins executing the correct thread. Compilers provide static branch prediction, setting a bit for the hardware. The 88110's target-instruction cache holds up to 32 double-instruction entries. Each entry caches the first two instructions for a taken branch of a loop. Loads are buffered and stores dynamically rescheduled to speed processing.

Graphics processing—The 88110 has 2 functional units for 3-D pixel processing, which includes shading, hidden-line removal, shading transformations, and lighting. Units take in 64-bit words with multiple pixels (4/8/16/32 bits/pixel) and operate on operand pixels in parallel. Instr include comparing Z-buffer values, packing/unpacking integer data into/from scan-line-order pixels, and rotating pixels for alignment.

Multiprocessing—The 88110 supports multiprocessing, has a built-in MESI cache-coherency protocol with hardware bus snooping. 88410 cache controller also handles multiprocessing for secondary caches.

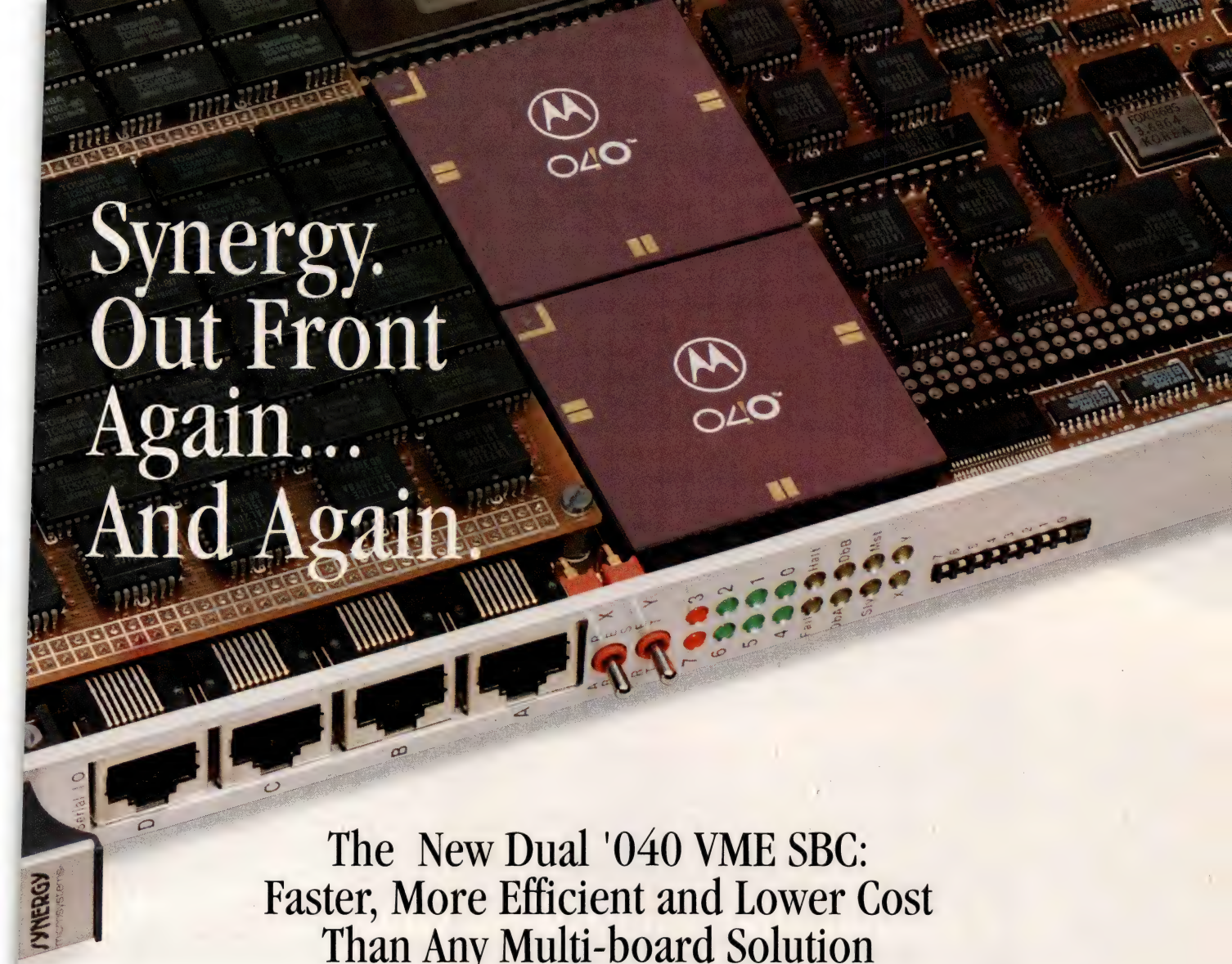
SUPPORT

□ HARDWARE

No hardware tools have yet been announced for the 88110. However, Tektronix (Beaverton, OR) supplies a logic analyzer for the 88100, and VMEtro (Houston, TX) has a specialized analyzer for the 88100. Motorola added JTAG and debug breakpoint registers to the 88110. A match on a logical address triggers a data-access exception. For debugging, the 88110 can be set for serial execution.

□ SOFTWARE

Both native and cross-development Unix-based tools are available for the 88100. Motorola has a 88110 development tool kit that includes a C compiler and a C-based 88110 simulator for the functional units, caches, and CPU internal states. The 88 Open Consortium (San Jose, CA), a private standards organization, has set up software portability standards and compatibility tests for the 88000 family. The 88000 has a good base of development tools and applications (see the 88 Open Sourcebook).



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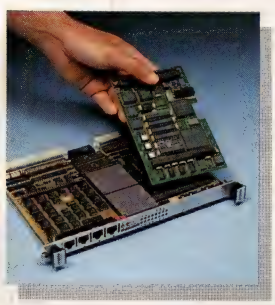

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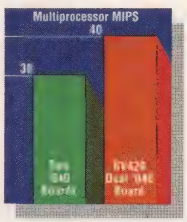

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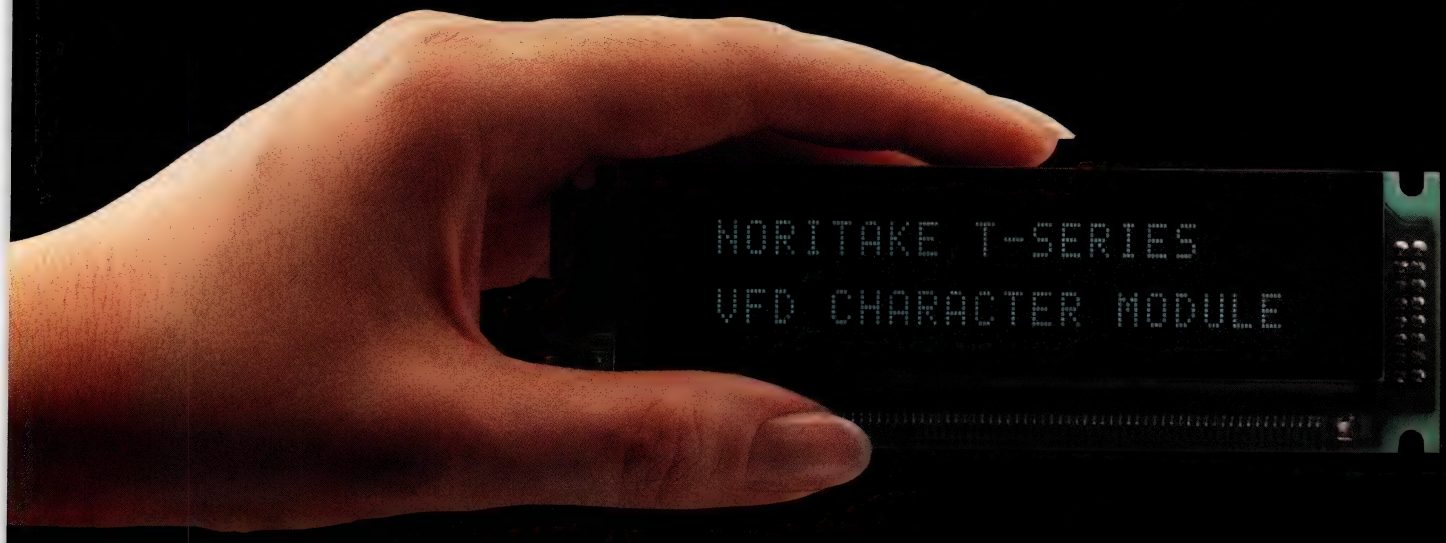

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CIRCLE NO. 81

SGS-Thomson Transputer

- 16-, 32-bit versions
- Stack-oriented CPU
- 3-reg stack, operand reg
- 2 reg pointers (workspace, PC)
- On-chip FPU (T805)
- 175 instr (variable length)
- Up to 4 kbytes on-chip SRAM workspace
- 32-bit multiplexed ext bus with refresh control
- 4 2-wire serial links to CPUs, I/O devices
- Hardware processes, tasks; 2 32-bit timers
- 2-D block-move instr
- T805 specs:
- 16/20/30-MHz internal clock (5-MHz ext)
- 33-nsec NOP (1 cycle)
- 233-nsec reg-mem ADD
- 1254-nsec MPY; 1287-nsec DIV
- 198-nsec floating-point ADD
- Floating-point ops: 594-nsec MPY; 924-nsec DIV
- 3-clock ext R/W
- 20-Mbps DMA-link transfer rate
- 1914-nsec intr latency

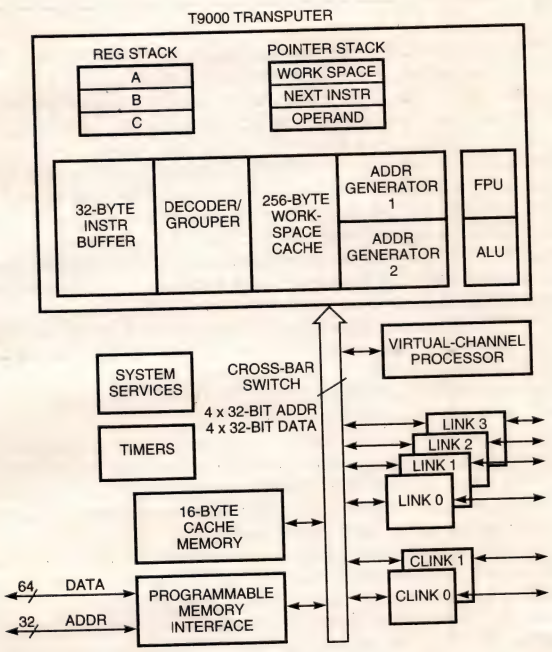
□ OVERVIEW

Introduced in 1986, the Transputer was one of the first 32-bit μPs and one of the last stack-oriented machines. A minimal, microcoded implementation, the Transputer was also the first μP specifically designed for multiprocessing—it has four serial 2-wire links for point-to-point CPU connections. The CPU has a 3-register stack, on-chip RAM (not cache), and no MMU. The Transputer initially had trouble getting a foothold in the market: It was ahead of its time in tackling 32-bit multiprocessing, and it was bundled with Occum, a new high-level, parallel-processing language. Since then, the Transputer has moved to standard languages like C and has built up a solid applications base, mainly in multiprocessing, that is unmatched by other μP. The 16-bit version is the T225; the 32-bit version with an on-chip 64-bit FPU is the T805. In 1993, SGS-Thomson will bring out a 40- to 50-MHz superscalar version that will deliver an estimated 71 SPEC89marks at 50 MHz.

□ VENDORS/PRICING

SGS-Thomson is the developer and sole supplier of the Transputer. IMST805 (30 MHz, PGA), $117; IMST400 (20 MHz, PLCC), $19; IMST225 (20/30 MHz, QFP), $13/$20.

ARCHITECTURE



Unlike most microprocessors, the Transputer is a stack-oriented machine. Instead of using a bank of general-purpose registers to hold local variables and interim processing results, Transputer processing revolves around a 3-register stack. A local on-chip SRAM workspace supplements the stack by holding other variables. The workspace is referenced by a workspace register.

The Transputer differs from mainstream processors in that it was designed for multiprocessing—applications and tasks running concurrently in more than one CPU. Each Transputer has two to four links—2-wire, serial ports for point-to-point links to other Transputer CPUs or I/O devices. These ports implement a byte-oriented protocol; they ship one serial byte plus a 2-bit header and trailer for each transaction. All communications are acknowledged via the second line. Each link has a raw bit capacity of 20 Mbps.

The Transputer was designed in conjunction with Occum, a parallel-processing language based on intercommunicating (nonblocked) processes. The CPU hardware schedules and maintains these processes. Processes can communicate via ports. The intercommunication between two processes is the same whether both processes run on the same CPU or on different CPUs. Communications between processes is either built into the high-level languages themselves, like Occum, or provided in libraries for languages like C.

Transputers are microcoded machines designed for high code density. Unlike most 32-bit processors, the basic instruction size is a byte. This 8-bit word is divided into op code and the operand. Additional instructions are added using the full 8 bits for the instruction op code and extending the instruction to sequential bytes. Also, a byte before the instruction—a prefix byte—can modify the instruction or build an immediate constant for it. One or more prefix bytes can also build up immediate operand constants in the operand register for the instruction. Up to 4 kbytes of on-chip SRAM supplies local fast memory, but the program must manage the memory.

Coming in 1993 is the T9000—a 50-MHz superscalar version of the Transputer. It keeps the basic Transputer ISA model and is code compatible. The T9000 has a 5-stage pipeline, 4 functional units, a process-based memory manager, a 32-word workspace cache for local variables, and a standard 16-kbyte on-chip cache. The functional units are an ALU, two address generators (instruction and data), and a 64-bit FPU. The T9000 also adds a programmable external-memory interface with a 64-bit data bus.

The T9000's upgraded serial links changed from the earlier point-to-point protocol to implementing a dynamic-switching, virtual-routing protocol. Links are now 4 wires—2 wires for each direction (signal+strobe). Max data rates are 20 Mbytes/sec per link. Packets can hold up to 32 bytes of data.

Processes—Built-in operating-system kernel schedules and times processes. Instr start, stop, and schedule processes. 2 operation-priority levels, each has its own scheduling timer. Lower-priority processes are scheduled as time slices; higher-priority tasks keep control until they relinquish it or time out. Tasks kept in linked list hardware maintains in memory.

Graphics instructions—Some CPUs have 2-D pixel block moves for graphics applications. Instr include 2-D block copy, 2-D block copy nonzero/zero bytes, and zero block.

□ VARIATIONS

IMST9000—New 32-bit superscalar Transputer. Pipelined operations with crossbar bus, RAM, new routed packet links. 50 MHz, 208-pin PGA.

IMST805—20 to 30 MHz, 32-bit CPU, 64-bit FPU, 4 kbytes SRAM, 4 links, graphics instr, DRAM controller, 84-pin PGA/PLCC, 100-pin QFP.

IMST400—Cost-reduced version. 20 MHz, 32-bit CPU, 2 kbytes SRAM, 2 links, graphics instr, DRAM controller, 84-pin PLCC, 100-pin QFP.

IMST425—20 to 30 MHz, 32-bit CPU, 4 kbytes SRAM, 4 links, DRAM controller, 84-pin PGA/PLCC, 100-pin QFP.

IMST225—20 to 30 MHz, 16-bit CPU, 4 kbytes SRAM, 4 links, 100-pin QFP, 68-pin PGA/PLCC. Nonmultiplexed bus: 16-bit data, addr.

Support chips—IMSC011: serial link to parallel bus or serial I/O; links μP or peripheral to a Transputer serial link. IMSC004B: 32-way crossbar.

Chip	Current (max at 5V)	Clock (MHz)
T805	240 mA	20
T425	200 mA	20
T225	140 mA	20

T805/425 in 84-pin PGA/PLCC; T225 in 68-pin PGA/PLCC.

SUPPORT

□ HARDWARE

SGS-Thomson and third-party vendors supply a wide range of development and evaluation cards for the Transputer. An ICE isn't available, but the Transputer's communications links provide a path to drive and monitor the CPU from an external host. Some CPUs have provisions for debug control. Additionally, many CPUs can boot up from a serial link, thus giving an external host control over the CPU for debugging.

□ SOFTWARE

Several development tool kits are available from both SGS-Thomson and third-party vendors. Languages such as C, C++, and Ada have been grafted onto the Transputer. Parallel-language development tools take advantage of the Transputer's process-oriented structure. These languages build code that can run in multiple CPUs.

☐ **OVERVIEW** Descended from Berkeley RISC 1 and II research, the 32-bit SPARC is the leading workstation/server μP. The SPARC design is a classic RISC architecture having a minimal instruction set, few addressing modes, hard-wired implementation, 3-address operations, and a load/store architecture. Initially, caches were offchip and unified, and CPUs lacked integer multiply and divide instructions. Later SPARC versions added a multiply instruction, and the latest superscalar versions have onchip caches. (Superscalar processors issue more than 1 instruction/cycle.) Sun Microsystems developed the SPARC for its systems and opened the architecture to chip and system vendors hoping to repeat the success of Intel's 80x86s in PCs. SPARC is now controlled by SPARC International (SI), an industry group; a license to build SPARC chips costs $99 from SI. Fujitsu sells a modified SPARC, the SPARClite (see entry), for embedded systems. The latest SPARC ISA version 9 from SI defines a 64-bit architecture with multiply and divide instructions.

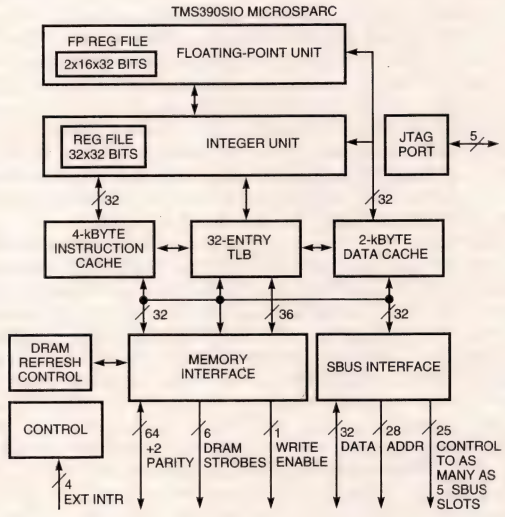
☐ **VENDORS/PRICING** Cypress, Fujitsu, LSI Logic, and Texas Instruments all build SPARC chips. LSI Logic uses a SPARC CPU as an ASIC core.

Cypress CY601A/02A (40 MHz, 207/144-pin PGA), $96/$150; Fujitsu MB86903 (40 MHz), $150; LSI Logic L64831 (40 MHz, 208-pir QFP), $168 (100); TI TMS390S10 (50 MHz, 288-lead TAB) $179.

SPARC

- Specs for TI MicroSPARC (TMS390S10):
- 32-bit SPARC μP, 120 regs with 7 reg windows
- 800,000 transistors
- 64-bit on-chip FPU, 16 64-bit regs
- 69 basic instr
- 5-stage pipeline
- 4-kbyte instr cache; 2-kbyte data cache
- Nonmultiplexed bus: 64-bit data, 31-bit addr
- SBus controller manages up to 5 devices on 32-bit bus
- DRAM controller handles 4 banks DRAM; refresh, programmable wait states
- Specs for TI MicroSPARC (TMS390S10):
- 50-MHz clock
- 1 instr/cycle execution (pipelined)
- 20 SPECint92; 15 SPECfp92
- 19-clock MPY; 39-clock DIV
- 4-clock floating-point ADD; 9-clock floating-point MPY
- 1-clock R; 2-clock W; 3-clock double store (60-nsec DRAM)
- 2-clock atomic R/W, SWAP
- 10-Mflops-pk FPU
- 7-clock typ intr latency

ARCHITECTURE



The SPARC is a classic RISC architecture descended from University of California at Berkeley RISC research and the RISC I and II chip implementations. As a classic RISC chip, the SPARC has a minimal architecture with few addressing modes and a small, simplified instruction set. Early RISC processors, SPARC CPUs have no integer MPY or DIV instructions.

Following Berkeley's lead, the SPARC processor is built around a large, multiple-ported register file. The register file breaks down into a small set of global registers for holding global variables and sets of overlapping register windows. Each 24-register window has a core of 8 registers supplemented by 8 registers overlapping the previous and next register windows. The overlapping registers eliminate the need to save and restore registers on function calls and returns or for context switches between tasks.

Initial SPARC implementations have a 4-stage pipeline: fetch, decode, execute, and write-back. Later chips, such as TI's MicroSPARC, expanded the pipeline to 5 stages by adding a memory stage to speed loads and stores. Following Sun's earlier workstation technology, SPARC chips used an off-chip physically addressed Sun Reference Model MMU.

SPARC International (SI), an industry organization, just released version 9 of the SPARC ISA. This version defines a 64-bit architecture with a lot of headroom for the future versions. Additionally, version 9 has full integer multiply and divide instructions as well as data prefetches to minimize cache misses, conditional register move , and branch prediction.

First-generation SPARC clock rates are now up to 50 MHz, the speed of TI's MicroSPARC. Later chips have cleaner memory interfaces and hardware requirements for exception processing. Today's SPARC chips require minimal system design. Chips such as the LSI Logic L64831 and Cypress CY601A integrate the integer CPU with an on-chip FPU with floating-point registers.

TI's MicroSPARC, introduced in late 1992, defines a new direction for second-generation SPARC processors: high-integration, low-cost, easy-to-design-in chips. Fitted with at least 4 kbytes of instruction cache and 2 kbytes of data cache, the MicroSPARC suits low- to mid-end desktop computing. A separate 64-bit memory interface handles up to 128 Mbytes of 16-Mbit DRAM. The processor also has an on-chip SBus interface and controller that can handle five SBus slots. The SBus is a 20-MHz, 32-bit synchronous bus.

MBus modules—Plug-in modules that interface to the MBus (40-MHz, synchronous, multiplexed bus: 36-bit addr, 64-bit data). These modules can have cache, as well as multiple processors. Superscalar SPARC implementations such as the TI SuperSPARC and Cypress hyperSPARC depend on MBus modules for high-performance off-chip cache.

SPARC chip sets—Available from Fujitsu, LSI Logic, Cypress, and Nimbus Technology. The chips sets provide all the logic and ext controllers needed to build a complete SPARC-based workstation. LSI and Cypress chip sets complement MBus-based modules. Nimbus has a chip set packaged with a mother board ready for insertion.

☐ VARIATIONS

Cypress CY601A/2A—Separate integer CPU and FPU chips. 25/33/40 MHz, 4-stage pipeline. Uses cache-controller chip.

Cypress SPARCset—Full SPARC chip set for MBus-based designs, CPU MBus module. Includes SBus, DRAM, graphics, DMA, and I/O controllers.

LSI Logic L64831—Integrated CPU, FPU. SPARC version 7, 25/33/40 MHz, 4-stage pipeline, 136 regs.

LSI Logic L64811/14—Integer CPU and FPU chips. 25/33/40 MHz, 136 regs, fast 8-clock intr response. 6 Mflops for FPU.

LSI Logic SparKit/MBus—Full SPARC chip set built around 40-MHz L64831. Uses MBus as main system bus. 6 chips plus CPU.

Nimbus SPARC board set—Full SPARC chip set and board ready for insertion. Uses same chips as Cypress SPARCset.

TI MicroSPARC (TMS390S10)—50 MHz, 4-kbyte instr cache, 2-kbyte data cache, 64-bit memory bus, SBus/DRAM controller, 288-lead TAE.

Chip	Current (max at 5V)	Package	Clock (MHz)
CY601A	600 mA	208-pin QFP	25
L64831	600 mA	280-pin QFP	40
MB86903	675 mA	207-pin PGA	40
TMS390S10	200 mA	288-pin TAB	50

SUPPORT

☐ **HARDWARE** ICEs and logic-analyzer pods are available for some of the SPARC chips. Check with the chip vendors for particulars.

See separate entries for Fujitsu SPARClite, TI SuperSPARC, and Cypress hyperSPARC.

☐ **SOFTWARE** All chips are SPARC ISA compatible and run Solaris operating software from SunSoft. There are more than 5000 applications for Sun SPARC-based systems, as well as development tools and operating software including real-time systems and kernels. Computer languages available for the SPARC include Fortran, Ada, C, C++, Lisp, Smalltalk, and Objective C.

Texas Instruments TMS340

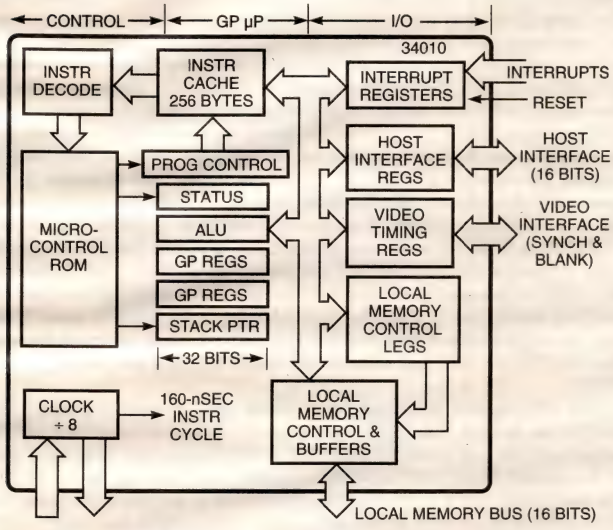
- 32-bit CPU; 32-bit data, ALU; 16-bit instr
- 170 instr
- FPU coprocessor
- 30 32-bit regs in 2 sets
- 512 bytes instr cache
- 512-Mbyte addr space
- Ext bus for DRAM, VRAM, refresh signals
- Pixel (x, y), linear bit addressing; 4-Gbit space
- 2/4/8/16/32-bit pixel sizes
- Graphics operations: clipping, lines, rotation
- Up to 60 MHz ext clock (34010), divide-by-4 internal
- 67/100-nsec pipelined reg-reg ADD, NOP (60/40 MHz)
- 3.7-μsec MPY, DIV (40 MHz)
- 2-cycle mem R/W (1 cycle in page mode)
- 50-nsec MPY-ACCUM in 40-MHz FPU
- 20-Mbyte/sec transfer; 32-bit host-CPU interface
- 4096×4096×24-bit CRT resolution (60 MHz)
- 2.7-μsec intr latency (48 MHz)

□ OVERVIEW Since its 1986 debut, Texas Instruments' TMS340x0 has built a large base in mid- to high-end graphics processing, especially in PCs. The 32-bit graphics processor combines single-cycle execution with hardware support for pixel addressing and operators for bit-mapped graphics. Designed as a graphics coprocessor, the 340x0 includes a host-CPU interface as well as VRAM and DRAM interfaces. The two generations are the initial 34010 and the later 34020, whose improvements include a larger 256-word instruction cache, additional operators, and a better memory interface. The 340X, a stripped-down version, finds employment in low-cost X terminals. Clock rates are up to 60 and 48 MHz for the 34010 and 34020, respectively. The internal clock rate is a quarter of the external rate and lets the 34020 deliver a pipelined average instruction execution of 83.3 nsec at 48 MHz. The TMS340x0 family supports the TIGA PC graphics standards.

□ VENDORS/PRICING Texas Instruments is the developer and sole source.

TMS34010 (40/60 MHz, PLCC) $20/$40; TMS34020 (32/50 MHz, PGA) $76/$132; TMS34020 (40 MHz, QFP), $60; TMS340X (40 MHz, QFP), $45.

ARCHITECTURE



Texas Instruments' TMS340x0 is a single-chip graphics coprocessor. The processor's operations for bit-mapped graphics include pixel addressing, pixel handling, line drawing, bit-blt moves, and clipping.

A register-based architecture, the 340x0 operates with two sets of 16 32-bit registers. One set functions as general-purpose registers. The registers in the second set are special-purpose registers that hold graphics-processing and system-configuration parameters. The registers are in the A and B register files, but the SP, PC, and status words are not in the files. The 34020 also has 54 16-bit registers that define peripheral control and I/O for DRAM, VRAM, and video-signal interfaces.

Engineers classify TMS40x0 family members as 32-bit processors with 32-bit registers, 32-bit internal data paths, and a 32-bit ALU. Instructions, however, are made up of one or more 16-bit words, and the multiplexed external bus may be 16 or 32 bits wide.

The 340x0 delivers single-cycle execution for most instructions executing from cache. However, the internal clock is 1/4 of the external clock, so the basic instruction rate is 12 MHz for a 48-MHz part. Execution slows for instructions executing from memory and for complex instructions.

The major 340x0 bottleneck is memory bandwidth—the amount of pixel or graphic data it can move in a given time. The 340x0 has a small on-chip instruction cache—512 bytes, which can make up 256 16-bit instructions or fewer for multiple-word instructions. This size is fine for graphics-algorithm inner loops given the CPU's compact graphics instructions. Thus, in an inner loop, the memory bandwidth can be dedicated to pixel manipulation, not instruction fetches. With a 10-MHz internal clock and a 2-clock memory cycle, pixel bandwidth pushes 20 Mbytes/sec, or 80 Mbytes/sec when setting 4 pixels to the same value in VRAM. According to TI, the 340x0 supports color and gray-scale CRTs with 1280×1024-pixel resolution and 256 colors/shades.

The TMS340x0's advantage is that it directly supports graphics processing, which simplifies graphics programming. The 340x0 CPU provides bit-level addressing to the pixel level. Programmers don't have to convert word- or byte-level code to find and handle bit-level data. The CPU addresses pixel data at the bit level, either as an X,Y display construct or as a linear stream of bits. Pixel sizes and display extents (screen sizes) are programmable via hardware registers. The same code can drive different-size CRT displays and pixels without changes, other than setting the defining hardware registers.

The following are 34020 instructions; some may not be in the 34010.

Graphics data types—Bit fields, bytes, pixels, pixel arrays. Bit addressing and X,Y addressing.

Line drawing—Inner loop of Bresenham line-drawing algorithm, fast line draw, set limits for line drawing, fill trapezoidal block with horizontal lines.

Pixel processing—Single-pixel draw and advance, pixel transfer, pixel block transfer, find equal pixel, replicate pixel, trapezoidal fill, pattern fill, fill pixel array, fill and pixel block transfer for VRAM. 16 Boolean and 6 arithmetic pixel-processing options (Raster ops).

Clipping—Pixel or bit in window or not, clip pixel array to fit window.

Special instructions—Block bit move, decrement reg and skip, jump, compare regs.

□ VARIATIONS

The 34020 has a memory controller with glueless interfaces for VRAM and DRAM including the controller refresh, 4 CAS (column-access-strobe) selects, and a page-mode (row and column) DRAM interface to minimize external logic. All chips interface to VRAM and video signals. The 34020 can directly address up to 1 Mbyte of VRAM and 4 Mbytes of DRAM.

TMS34010—First generation, up to 60 MHz; 128-word instr cache, pixel depth to 16 bits, 68-pin PLCC.

TMS34020—Second generation, up to 48 MHz, 256-word instr cache, pixel depth to 32 bits, hardware emulation support, 145-pin PGA, 132-pin QFP. Interfaces to FPU, other 340x0s for multiprocessing.

TMS340X—Stripped-down 34020 for X-terminals, 256-word instr cache, 144-pin QFP. No coprocessor, host, or multiprocessor interface.

TMS34082 FPU—32/40 MHz, 50-nsec MPY-ACCUM at 40 MHz, 22 64-bit floating-point regs, 8 control regs, 2-item operation stack. 32-bit integer and single-precision floating-point ops; 64-bit, double-precision floating-point ops.

Chip	Current (max)	Voltage (V)	Clock (MHz)
34010	175 mA	5	60
34020	140 mA	5	40

34010 in 68-pin PLCC; 34020 in 145-pin PGA.

SUPPORT

□ HARDWARE The 34020 has a 4-wire emulation-support interface. Through these lines you can control CPU execution, set breakpoints, and read/write memory or registers. TI sells an ICE for the TMS340 family and offers a "scan-based" emulator that uses the serial test port to control and monitor the processor. Hardware evaluation boards are also available.

□ SOFTWARE TI provides an assembler/linker, C compiler, and C source debugger for the TMS340 family. TI also has a graphics library with common graphic functions. Development tools include a software porting kit, software developer's kit, and driver development kit for the TIGA graphics standard.

□ OVERVIEW

Second-generation RISC processors are moving towards multiple-instruction issuance for higher performance. TI's SuperSPARC is the first superscalar SPARC implementation—it can issue up to 3 instructions each clock cycle. Designed by Texas Instruments and Sun Microsystems, the 3.1M-transistor SuperSPARC integrates 20 kbytes of instruction cache, 16 kbytes of data cache, an MMU, and on-chip floating-point execution units. At its mid-1992 introduction, the SuperSPARC had the largest on-chip cache for a RISC μP. Running at 40 MHz, the SuperSPARC delivers 52-SPECint92, 65-SPECfp92 performance. The processor's eight functional units include three integer ALUs (two are separate or feed the third) that can execute concurrently. A secondary-cache controller comes in MBus modules or as a separate chip. The modules plug into the standard SPARC International MBus—a 40-MHz, synchronous, multiplexed bus (36-bit address, 64-bit data).

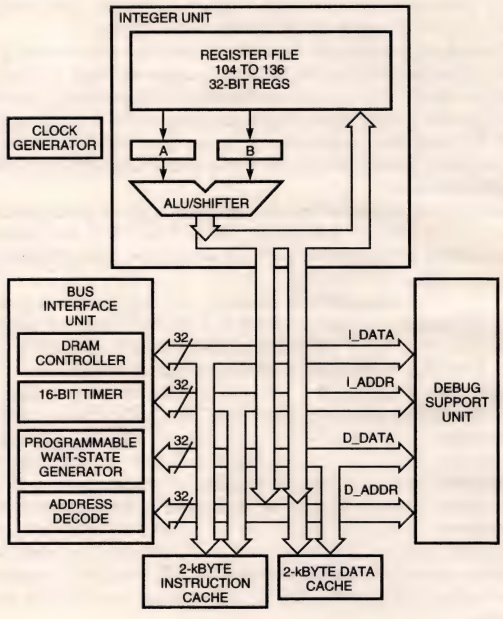
□ VENDORS/PRICING

Texas Instruments developed the SuperSPARC with Sun Microsystems and is the sole supplier. SuperSPARC (33/36/40 MHz), $949/$1199/$1899 (1000); SuperSPARC MBus modules (33/36/40 MHz), $1149/$1399/$2099 (1000).

Texas Instruments SuperSPARC

- 32-bit SPARC RISC μP; 136 regs, on-chip FPU
- 3.1M transistors (BiCMOS)
- 108 instr
- Superscalar, 8 functional units
- 20-kbyte instr cache
- 16-kbyte data cache
- 8-stage pipeline (1/2 clock/stage)
- 4-entry branch-target queue
- VBus, MBus ext interfaces; 36-bit addr, 64-bit data
- MBus module: CPU, cache controller, caches
- 33/36/40-MHz clock
- Issues up to 3 instr/clock
- 52 SPECint92, 65 SPECfp92 (40 MHz, 1-Mbyte ext cache)
- Up to 3 ALU instr/cycle
- Pipelined FPU, ADD, MPY units; 3-clock latency
- 128-bit-wide instr cache for multiple-instr fetch
- Branch-delay slot
- Buffers 8 double stores
- VBus module runs at CPU clock rate; MBus at 40 MHz

ARCHITECTURE



TI's SuperSPARC is the first superscalar SPARC implementation. This huge chip holds 36 kbytes of cache memory as well as floating-point functional units. The SuperSPARC can issue up to 3 instructions per cycle, moving the selected instructions as a group through the logic. Initial clock rates are 33 to 50 MHz, scalable to 100 MHz over time. At 40 MHz, the SuperSPARC achieves 52-SPECint92, 65-SPECfp92 performance—basically equivalent VAX performance in MIPS for integer and floating-point applications, respectively.

Operations center around the 136-entry, 8-ported register file. Registers are grouped into 8 global registers and 8 overlapping register windows. The register file handles 6 reads (3 2-operand reads) and 2 writes (2 third operands). Actually, the file can perform 2 reads and 2 writes concurrently but is time-shared to handle 6 reads and 2 writes in 1 system-clock cycle.

The SuperSPARC doubles the system clock to run its pipeline stages. The eight stages are grouped into four execution stages—fetch, decode, execute, and write-back—of different lengths. The eight stages are cache access, send matched instructions to scheduler (F0, F1); issue instructions (1, 2, or 3), read address registers/evaluate branch-target address, read operands from register file (D0, D1, D2); first, second ALU stages (E0, E1); and write-back result (WB).

The CPU runs 8 functional units. These units include 3 integer ALUs, load/store, branch, floating-point multiply, floating-point add, and shift. The adder units are organized so two can execute concurrently and return results to the register file or feed into the third ALU. That ALU can then operate on the results and return a value to the register file in one pipeline cycle. Thus, the SuperSPARC can do three adds in one cycle, where one add is dependent on the first two results. The multiply and add floating-point units are pipelined—they can accept a new instruction every clock cycle but have a 3-cycle latency. The FPU has its own instruction queue and 16 64-bit registers. It does single- and double-precision IEEE-standard floating-point operations.

The SuperSPARC has large on-chip caches to boost performance and minimize cache misses. The larger caches also maximize the effect of superscalar operation by having more instructions available on chip. The 20-kbyte instruction cache is 5-way set associative; the 16-kbyte data cache is 4-way set-associative. The CPU addresses both caches physically. The cache instruction path is 128 bits (4 words wide) to handle superscalar operation. Four instructions are presented at a time to the 8-deep prefetch queue.

The data cache can operate in either write-back or write-through mode. Access time is 11 nsec, which lets the CPU use a cache hit in the next cycle. A single TLB supports both caches. It has 64 entries and does two TLB evaluations in one clock cycle.

The SuperSPARC runs in stand-alone mode by interfacing to the MBus. The processor can run in cache-controller mode by interfacing to an external cache controller via the VBus—a nonmultiplexed, proprietary bus (CPU clock rate, 36-bit address, 64-bit data). The VBus links to a cache controller and up to 2 Mbytes of unified secondary-cache SRAM. The cache controller can handle multiprocessing (more than one SPARC CPU on an MBus).

Branch-delay slots and a branch-target queue minimize branch penalties. A branch-delay slot following the current set of instructions gives the hardware the time to prefetch both the target set and the next sequential set of instructions.

□ VARIATIONS

TMS390Z50 SuperSPARC—Superscalar SPARC μP, issues up to 3 instr/clock. 33/36/40 MHz, 20-kbyte instr cache, 16-kbyte data cache.

TMS390Z55 cache controller—Can link module CPU via VBus to MBus. 33/36/40 MHz, 339-pin PGA, handles up to 1 Mbyte of cache.

TMS390Z50-XXV module—MBus module with SuperSPARC CPU, cache controller, 1 Mbyte of pipelined SRAM cache. CPU speed is 33/36/40 MHz.

Chip	Current (max at 5V)	Clock (MHz)
TMS390Z50	1.7A	40
TMS390Z55	1.2A	40
Module	4.0A	40

TMS390Z50 in 293-pin PGA;
TMS390Z55 in 396-pin PGA.

SUPPORT

□ HARDWARE

Using the JTAG port, you can set breakpoints, single-step execution, and monitor or change memory or register data. A breakpoint register matches on a 32- or 36-bit code or data address. Address bits can be masked for larger address ranges. Two 16-bit counters handle instruction and cycle counts. A software instruction lets the SuperSPARC enter emulation mode. Special pins detail pipeline operation. Logic analyzers can use the strobe pin.

□ SOFTWARE

The SuperSPARC is compatible with existing Sun operating software and SPARC development tools. TI furnishes a SuperSPARC simulator—SPARCsim—that simulates instruction execution as well as the effects of cache, MMU, and store buffers. A Verilog HDL model of the chip and cache controller is available as is the SuperSPARC Scantool for controlling board- and system-level test via the JTAG port.

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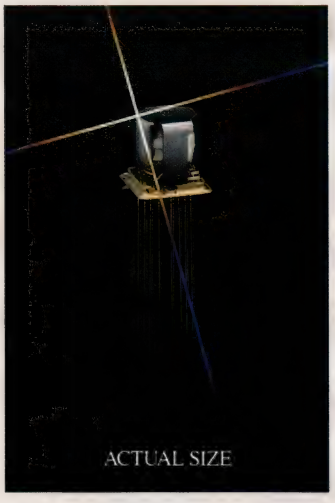

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☐ **OVERVIEW** The Mips R4000 is the first 64-bit RISC μP. Originally running at 50 MHz, the R4000 doubled Mips R3000 performance. With an 8-stage, 100-MHz pipeline, the R4000 can start an instruction each clock cycle if there are no interlocks or data dependencies. Two 8-kbyte on-chip primary caches speed performance, and a new memory interface eliminates the R3000's need for dual external caches running at twice the system clock rate. The three R4000 versions range from the PC, which has no external cache, to the MC, which supports an external cache and multiprocessing. The R4000A upgrade, announced in November 1992, boosts cache sizes to 16 kbytes each, raises clock rates to 66.7 and 75 MHz, and uses 3.3V for lower power consumption. Low-end variations of the R4000 for PCs and portable and embedded systems will start emerging in 1993.

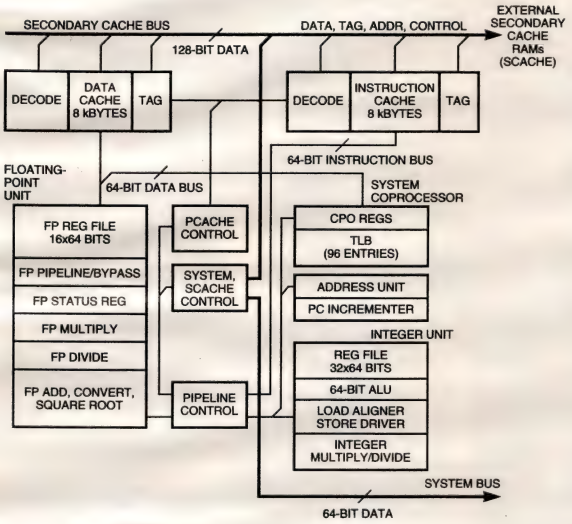
☐ **VENDORS/PRICING** Mips Technologies Inc, now part of Silicon Graphics, developed the Mips R4000 architecture and licenses it for manufacturing to Integrated Device Technology, LSI Logic, NEC, Performance Semiconductor, Siemens, and Toshiba. Some vendors, such as IDT, can also modify or build new Mips R4000 designs.

IDT R4000PC/SC/MC (50 MHz), $750/$900/$950 (1000); NEC R4000PC/SC, $600/$800 (50,000); Performance Semiconductor R4000PC/SC, $700/$850 (1000); Siemens R4000PC/SC, $1050/$1250 (1000); Toshiba R4000PC/SC/MC, $700/$810 (1000).

Mips R4000

- 64-bit RISC μP, 32 64-bit regs
- On-chip FPU, 16 64-bit regs
- 1.7M transistors (R4000A)
- 133 instr
- Superpipelined
- 8-stage pipeline (1 stage/internal clock)
- 16-kbyte instr, data caches; up to 4 Mbytes ext secondary cache (128-bit bus)
- 64-bit virtual-addr space, 36-bit physical-addr space
- Multiplexed ext bus: 36-bit addr, 64-bit data (R4000SC)
- 1 ext intr (8 intr total)
- 50-MHz ext clock (100-MHz internal clock, or pclock)
- R4000A has 66.7/75-MHz ext clock
- 57.6 SPECint92, 60.3 SPECfp92 (with 1-Mbyte ext cache at 50 MHz)
- 1 internal clock/instr execution (pipelined)
- Superpipelined: starts instr on every internal clock (every pclock)
- 20-pclock MPY; 133-pclock DIV
- 3-pclock branch delay; 2 load/use delay slots
- 2-ext-clock mem R/W
- 4/8/16/32-word bursts (1 clock/burst cycle)

ARCHITECTURE



The R4000 is the next step up for the Mips RISC architecture. It more than doubles Mips R3000 CPU performance and sets the direction for Mips μPs for the rest of the decade. Moreover, the R4000 is a significant step for RISC architectures: It's the first 64-bit μP.

Building on the classic Mips RISC architecture, Mips engineers raised performance by cranking up internal clock rates to 100 MHz (150 MHz for the R4000A) and superpipelining the R4000 implementation. All functional units are pipelined; each stage runs at twice the system clock. Instruction fetch, for example, goes from 1 pipeline stage in the previous R3000 to two stages in the R4000. The advantage of this superpipelining is that a new instruction can start on every half system clock—virtually doubling instruction issuance over earlier Mips systems.

Instruction issuance doesn't actually double because of pipeline hazards and data dependencies. But the combination of superpipelining and faster clocks more than doubles performance over previous Mips generations. And the combination is scalable—reaching 250 MHz.

The R4000's pipeline was extended to 8 stages from the R3000's 5 stages. The R4000 stages are instruction fetch (1st half), instruction fetch (2nd half), register file (access), execute, data cache (1st half), data cache (2nd half), tag check (check TLB tag), and write-back. An instruction can start on each internal-clock (pclock) cycle. The pipeline incurs a 3-cycle delay before a branch is executed. The compiler fills these 3 slots with NOPs or instructions for the current thread. There is a 2-cycle load delay.

The R4000 added two 8-kbyte on-chip caches for code and data to keep the pipeline filled. The R4000A cache sizes are 16 kbytes each. These caches and the improved memory interface remove the major design barrier that limited earlier Mips processors. Older Mips processors needed dual off-chip caches for high performance. These caches ran off a single time-multiplexed bus, and each cache was accessed at twice the system clock rate. This dual-cache/bus arrangement caused Mips CPUs to top out at 30 to 40 MHz because they were limited by the 60- to 80-MHz rate for cache accesses.

The R4000 implements the Mips III ISA, a superset of earlier Mips architectures. Mips III introduces new instructions, primarily double-word loads, stores, shifts, and add/sub. These double-word instructions take advantage of the R4000's 128-bit secondary-cache bus and 64-bit system bus. The R4000 addresses a 64-bit virtual-address space. However, that 2^{64} space is mapped into a smaller 2^{36} physical space.

64-bit processing—The R4000 has a 64-bit-wide CPU and ALU and 64-bit regs and data paths. It handles 32-bit programs and data by sign-extending regs. There are some necessary 64-bit instructions. The on-chip FPU performs 32-bit single-precision and 64-bit double-precision floating-point operations and is compatible with earlier Mips FPUs. Integer multiply and divide are done stepwise in bit pairs and single bits, respectively. The chip handles both 32- and 64-bit multiplies and divides. 32-bit arithmetic results can be used seamlessly in 64-bit computations. You don't have to track operands and specify conversions.

☐ **VARIATIONS**

The R4000 has three chip variations. All contain the core R4000 CPU, 2 8-kbyte caches, and an on-chip FPU. All run at 50 MHz.

R4000PC—Basic R4000 packaged for low-end systems. Runs with on-chip cache only. 179-pin PGA.

R4000SC—Basic R4000, can run with up to 4 Mbytes of secondary ext cache. Has 128-bit-wide interface for ext cache. 447-pin PGA, LGA.

R4000MC—R4000 CPU with secondary-cache controller and multiprocessing capability; otherwise, same features as R4000SC. Optional bus-snooping or directory-based cache-coherency schemes. 447-pin PGA, LGA.

R4000APC/SC/MC—New version of R4000, has same 3 variations. Runs at higher clock rates (66.7/75 MHz) and has larger, 16-kbyte caches.

Chip	Current (max at 5V)	Package	Clock (MHz)
R4000PC	2.2A	179-pin PGA	50
R4000SC	2.4A	447-pin PGA	50
R4000MC	2.4A	447-pin PGA	50

SUPPORT

☐ **HARDWARE** The R4000 has a watch-breakpoint debugging register to break on references to a selected physical address. The chips have JTAG ports for board and chip testing. The R4000SC has a low-speed serial interface to configure the CPU at boot time and a programmable secondary-cache controller for booting up. Embedded Performance (Santa Clara, CA) has an ICE for the R4000, and several logic analyzers are available for the CPU.

☐ **SOFTWARE** The R4000 can use the development, operating, and applications software for the R2000/3000 line. Mips and the chip vendors offer a development package with system simulators, cache design/optimization tools, PROM monitor, code profiler, and debugger. Unix and real-time operating systems are also available for the R4000. Microsoft's soon-to-emerge Windows NT will run on the R4000, which means that the chip will be able to run future and existing Windows applications.

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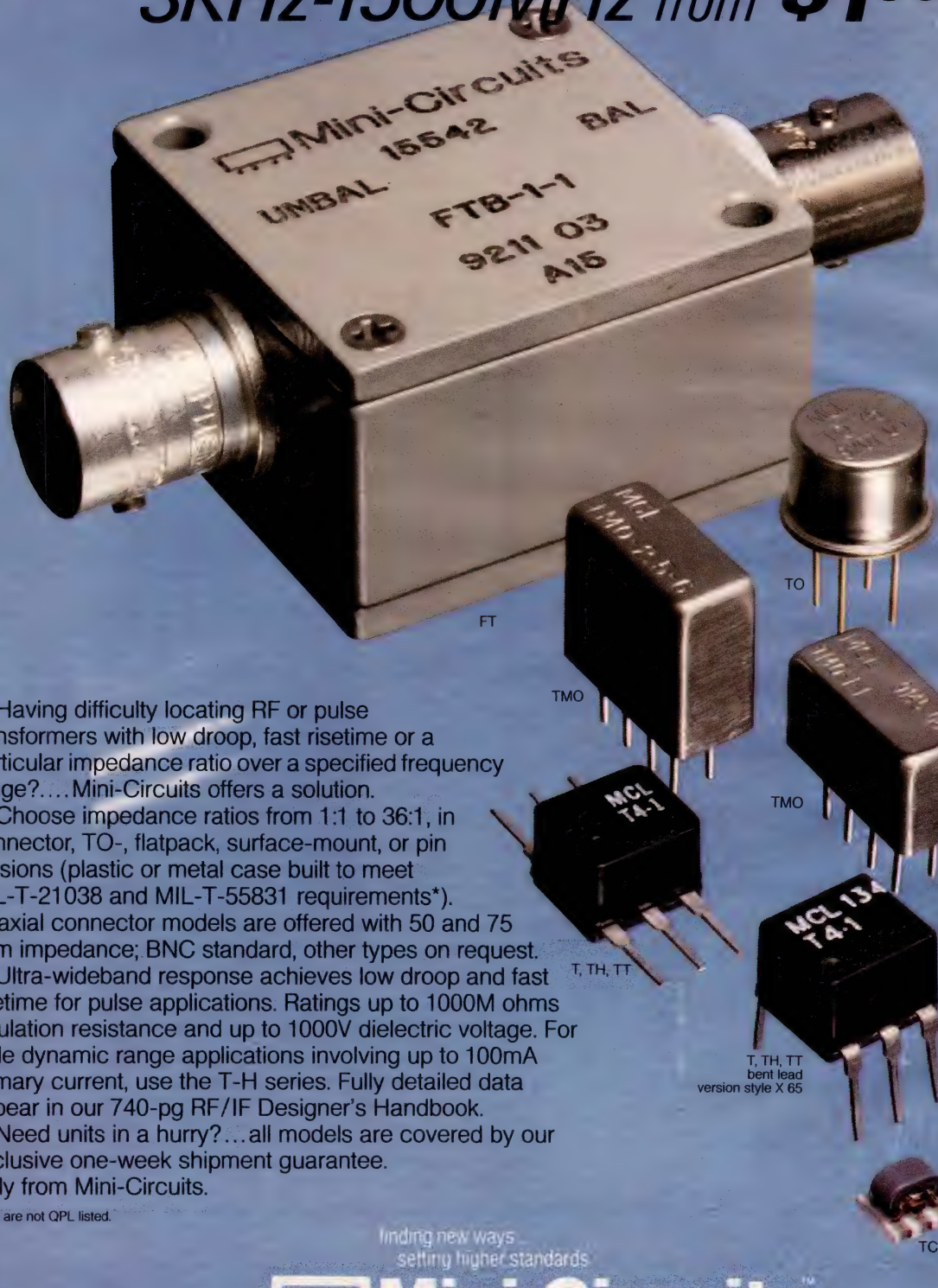

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CIRCLE NO. 66

F71 REV. D

Micropower cell doubler operates down to 0.9V

Koen Weijand, Bakken Research Center, Maastricht, The Netherlands

The circuit in **Fig 1** operates from a 1.5V cell and produces a ±1.5V output. The 74HCT4053 triple, 2-channel analog multiplexer operates as a charge pump and oscillator. Pump capacitor C_1 alternatively charges up to the 1.5V battery and discharges to the negative-rail storage capacitor, C_3. Switches X and Y perform the charge-pump action. The circuit configures switch Z as a self-oscillator that functions as an inverter with RC feedback through R_1 and C_2. The in-phase signal at node Y drives the other end of C_2 to invoke Schmitt-trigger action.

Using the standard CMOS 74HCT4053, the circuit self-starts from 0.9V. At 1.5V, the circuit's quiescent current is less than 0.5 µA, using **Fig 1**'s component values. Increasing the value of C_2 will produce an even lower idle current drain for those who need only a voltage and low output current. For input voltages lower than 0.9V, the negative output voltage can drive the logic. In that case, V_{SS}, INH, and Z_1 should connect to V_{EE} instead of the minus battery terminal.

Using the HCT version of the 74HCT4053 reduces the current drain of the oscillator because of this version's asymmetrical switching thresholds, which cause an asymmetrical duty cycle. For those applications that need the lowest output impedance, rather than the lowest idle current, you can use the HC version at a higher frequency and with a larger C_1. The lower limit of the output impedance is set by the switch resistances plus T/C dynamic performance, where 2T = 1/f (f = frequency) and C = pump-capacitor value, C_1.

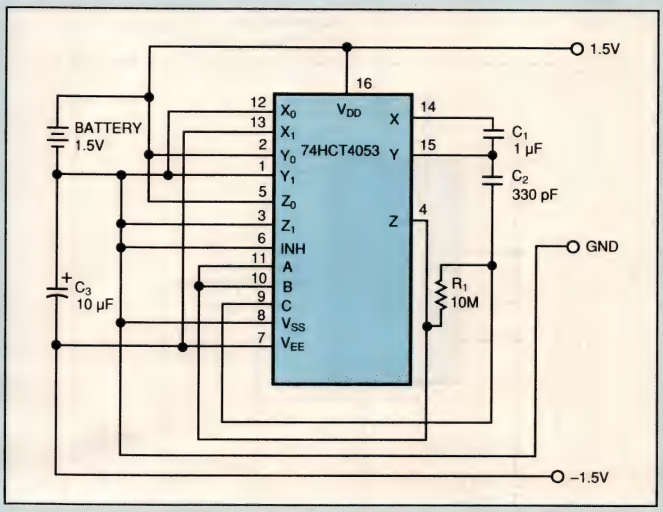

Fig 1—Producing ± 1.5V from a 1.5V cell, this cell doubler draws a quiescent current of less than 0.5 µA and operates at voltages as low as 0.9V.

EDN BBS /DI_SIG #1165

To Vote For This Design, Circle No. 361

LED signals lamp failure

Chester Simpson, National Semiconductor, Santa Clara, CA

Although incandescent lamps are visible regardless of surrounding lighting conditions, their main drawback is limited reliability. Sooner or later, all incandescent lamps will fail when their filaments burn out due to the extreme temperature transitions of going from cold to glowing hot. For cases in which the lamp serves as a critical warning, **Fig 1**'s circuit uses an LED status indicator that provides three types of information about the incandescent lamp and its drive circuits:

- If the LED indicator is dark, the lamp filament is OK and the lamp-activator switch is not closed.
- If the LED glows steadily, the lamp-activator switch is closed and the voltage supply to the lamp socket is OK.
- If the LED is flashing, the lamp filament has blown open or the lamp is disconnected from the socket, and the lamp-activator switch is not closed.

The circuit operates by relying on an incandescent lamp's cold resistance, which, in a good lamp, is low, typically less than 20Ω. If the lamp burns out and the filament opens, the resistance is then infinite. This large change in resistance controls the operation of the status-indicator LED.

The circuit utilizes a 555 timer operating as a free-running oscillator that runs at about 3 Hz. The output

Text continued from pg 163

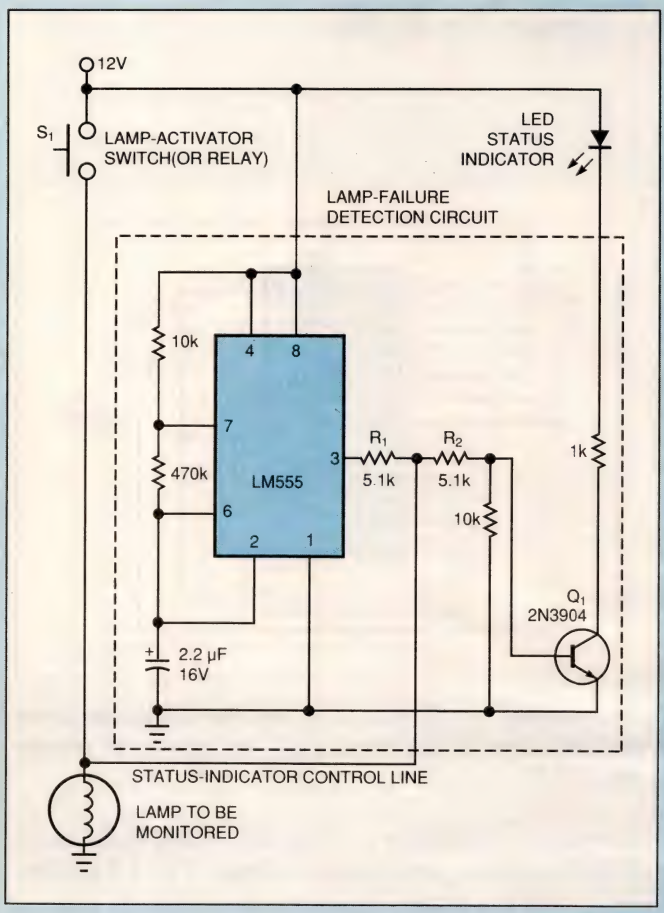

Fig 1—The lamp's impedance—low while the bulb is good but high when blown out—controls this lamp-failure detection circuit's 555 timer, which in turn controls the action of an indicator LED.

of the 555 timer oscillates from high to low at the 3-Hz rate any time the 12V rail is applied to pins 4 and 8. While the bulb is good, the low impedance presented by the lamp filament keeps the output of the 555 from activating Q_1 and thus prevents the LED from flashing by holding the R_1/R_2 junction near ground. If the bulb's filament blows open, the output of the 555 then drives Q_1 through R_1 and R_2, causing the LED to flash at the 3-Hz rate. This flash provides immediate warning to the operator that the lamp has failed.

The LED indicator also turns on whenever the lamp-activator switch is closed, thereby applying 12V to the lamp. This 12V will turn Q_1 on by holding the R_1/R_2 junction at 12V, causing the LED indicator to glow steadily. This steady glow indicates that voltage is being applied to the lamp, ensuring the proper operation of the switch and verifying that there is no short to ground at the lamp socket.

EDN BBS /DI_SIG #1166 EDN

To Vote For This Design, Circle No. 362

Integer trig functions execute quickly

Brian Dombrowsky, Prince Machine Corp
Holland, MI

The integer-math, C trigonometric functions in **EDN BBS /DI_SIG #1144** run significantly faster than floating-point ones.

To Vote For This Design, Circle No. 363

TSR dumps video buffer to COM port

K V Ramakrishnan, DRDO-NPOL
Cochin, Kerala, India

The TSR (terminate-and-stay-resident) program in **EDN BBS /DI_SIG #1125** will dump a PC video buffer's contents to a terminal connected to COM1 or COM2.

To Vote For This Design, Circle No. 364

Program sizes voltage dividers

John Dunn
Merrick, NY

The GW-Basic program in **EDN BBS /DI_SIG #1108** accepts your voltage specifications and calculates the values for a resistor string. You can also specify total resistance for the string.

To Vote For This Design, Circle No. 365

C function converts floating point to ASCII strings

Rémy Point, École Centrale de Lyon
Ecully, France

Similar to C functions itoa(), ltoa(), and utoa(), the C function ftoa() in **EDN BBS /DI_SIG #1095** converts floating-point numbers into ASCII strings.

To Vote For This Design, Circle No. 366

These Software Shorts listings are too long to reproduce here. You can obtain the listings from the Design Idea Special Interest Group on EDN's bulletin-board system (BBS): (617) 558-4241, 300/1200/2400/9600 8,N,1. From Main Menu, enter ss/DI_SIG, then rk*nnnn*, where *nnnn* is the number referenced above.

LINEAR TECHNOLOGY

DESIGN NOTES

RS232 Transceivers for Hand Held Computers Withstand 10kV ESD – Design Note 64

Sean Gold

Battery-powered computers and instrumentation are often subjected to severe electrical stress which imposes some stringent demands on serial communication interfaces. As always, operating from a battery mandates minimal power consumption. Transceivers must also tolerate repetitive Electrostatic Discharge (ESD) pulses because cable connections frequently come in contact with humans and other charged bodies.

Linear Technology's LT1237 addresses the above requirements. The LT1237 is a complete RS232 port, with three drivers, five receivers and a regulated charge pump. Supply current is typically 6mA, but the device can be shut down with two separate logic controls. The driver disable pin shuts off the charge pump and the drivers – leaving all receivers active, I_{SUPPLY} = 4mA. The ON/$\overline{OFF}$ pin shuts down all circuitry except for one micropower receiver, I_{SUPPLY} = 60µA. The active receiver is useful for detecting start-up signals. The LT1237 operates up to 120kBaud and is fully compliant with all RS232 specifications. Connections to the RS232 cable are protected with internal ESD structures that can withstand repetitive ±10kV human body model ESD pulses.

Figure 1 shows a typical application circuit. The LT1237's flow through pinout and its ability to use small surface mount capacitors, helps reduce the interface's overall footprint.

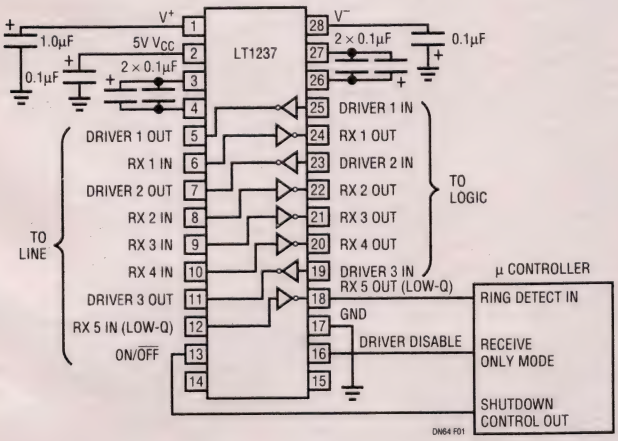

Figure 1. LT1237 Application Circuit

Interfacing with 3V Logic

Hand held computers are rapidly moving to 3V logic to save power. Yet higher voltage buses are still utilized elsewhere in the system for display driving and other functions. The LT1330 is functionally equivalent to the LT1237 but operates from 5V with a separate logic supply to interface directly with 3V logic. (Figure 2)

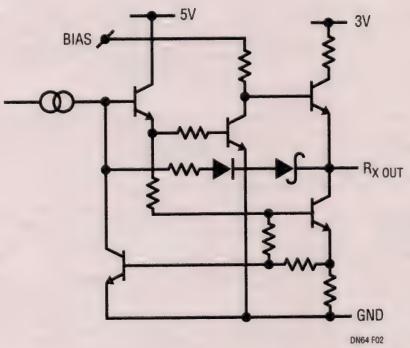

Figure 2. Receiver Output Stages in the LT1330 are Biased From a Separate Logic Supply to Easily Interface with 3V Systems

ESD Protection Techniques

Even though the I/O pins on the LT1237 and LT1330 are protected, a basic understanding of electrostatic discharge, its causes and its remedies, is helpful when designing with these circuits.

ESD generated by triboelectric charging of the human body is often the most troublesome problem for portable computers.[1] Energy imparted during a discharge is usually in the form of a rapidly rising high voltage pulse with a slow exponential tail. ESD pulses can be modeled with the switching circuit shown in Figure 3. ESD contributes frequency components well into the GHz range. At such frequencies, nearby cables and PC board traces look like receiving antennas for ESD noise.

1. Triboelectricity is the charge created as a result of friction between bodies.

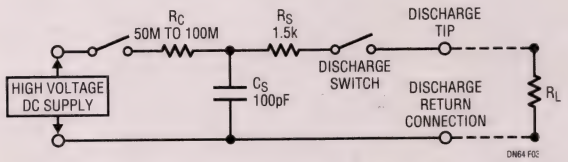

Figure 3. Human Body Circuit Model for ESD Pulses

Circuit damage from ESD can occur as a result of three effects: (1) High current heating, which destroys junctions or metallization. (2) Intense electromagnetic fields, which break down junctions or thin oxides. (3) Radiated noise, which drives the circuit into invalid or locked up states.

Any action which eliminates the charge generator, circumvents charge transfer, or enhances the circuit's ability to absorb energy, will increase a circuit's tolerance of ESD. Eliminating the ubiquitous charge generators and disrupting charge transfer are difficult tasks because they demand strict control of the circuit's operating environment. A more practical approach is to limit ESD entry points by shielding the circuit's enclosure and covering the RS232 port's connector when it is not in use.

Another practical remedy is to increase a transceiver's ability to absorb energy by clamping the RS232 line to ground with fast acting avalanche diodes or dedicated transient suppressors (Figure 4). Discrete suppressors are widely available and are extremely effective. Designers are often reluctant to use discrete suppressors because they are expensive. Costing up to $0.40/pin, they can sometimes exceed the cost of the transceiver.

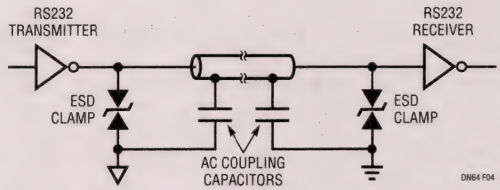

Figure 4. Older Interface Designs Used External ESD Clamps

The LT1237 and LT1330 incorporate the clamps for diverting ESD energy on chip. These active structures quickly respond to positive or negative signals at threshold voltages higher than RS232 signals, yet below destructive levels for the device. The path of high current flow is through large pn junctions which increases the capacity to absorb energy.

When a discharge occurs, the resulting current flow is insignificant when the transceiver is turned off or powered down. When operating, the resulting current may debias internal circuitry and lock up the circuit. Observations have shown these nondestructive errors to be highly dependent upon the logical state of the transceiver. Cycling the power clears the circuit.

When very high levels of ESD protection are required, an external LC filter (Figure 5) can be used to drop ESD energy into a range that can be safely dissipated within the transceiver.

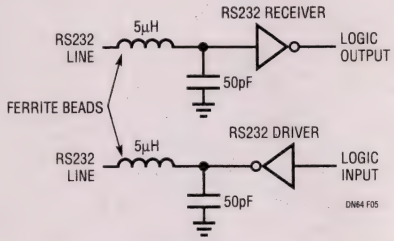

Figure 5. External LC Filters Provide Protection From Very High Levels of ESD Yet Cost Less Than Discrete Supressors

PC Board Layout

Energy shunted through an ESD clamp can still cause problems if the impedance of the return path is large enough to create a sizable voltage drop. Such voltage drops may damage unprotected components that share the common return line. Including a low inductance ground plane in the PC board is therefore essential for good ESD protection. For the LT1237 and LT1330, the AC path to ground through V^- must also be low impedance. Adding a few hundred picofarads of low ESR capacitance in parallel with the primary storage capacitor provides a good AC ground.

When using discrete transient suppressors or filters, place components as close as possible to the connector with short paths to the return plane. Make the spacing between the circuit board traces as wide as possible. ESD pulses can easily arc from one trace to another when the spacing between traces is narrow. Arcing occurs slowly compared with ESD rise time, so air spark gaps alone will not protect circuitry from ESD. Dedicated spark gaps are effective for limiting ESD energy when used with additional suppression devices.

Do not float the cable shield with respect to local ground. Designers may feel inclined to do this to avoid circulating current due to differences in ground potential. Instead, AC couple the grounds so they are shorted at ESD frequencies.

Conclusion

The techniques described here cannot entirely eliminate ESD problems, but understanding ESD's nature and using careful circuit design, will help protect against its intrusion.

For literature on our family of RS232 transceivers, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456

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LT/GP 1192 190K

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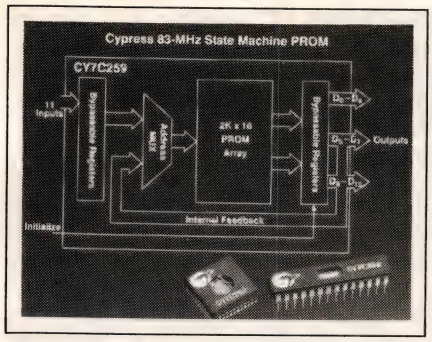
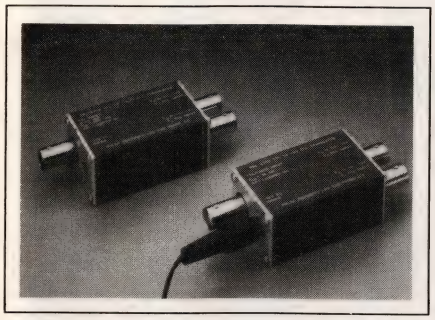


State-machine PROMs. The 83-MHz CY7C258/9 PROMs implement 2048 states in a 2k × 16-bit PROM array. The chip's architecture internally feeds back 11 of the 16 array outputs. The remaining five array outputs are dedicated outputs on the chip. You can change the setup and hold time of the input registers and can bypass the input and output registers to allow synchronous or asynchronous operation. CY7C258, in 28-pin PLCCs (plastic leaded chip carriers), $29.05; CY7C259, in 44-pin PLCCs, $40.60 (100). **Cypress Semiconductor Corp,** 3901 N First St, San Jose, CA 95134. Phone (408) 943-2600. **Circle No. 419**

3V dual op amp. The OP-295 is a dual op amp that operates on 3 or 5V. The maximum offset voltage is 500 μV, and the maximum supply current is 300 μA. When driving a 10-kΩ load from a 3V supply, the output swing is a minimum of 2.9V. Other specifications include a voltage-offset drift of 1 μV/°C and a noise-voltage density of 53 nV/√Hz. Typical gain-bandwidth product is 75 kHz. $1.98. **Analog Devices,** One Technology Way, Box 9106, Norwood, MA 02062. Phone (617) 329-4700. FAX (617) 329-1241. **Circle No. 420**

Field-programmable gate arrays. The CLi6000 series of FPGAs have as many as 5000 gates. They operate as fast as 70 MHz and have flip-flop toggle rates of 150 MHz. Typical operating current is between 50 and 70 mA. Standby current is 500 μA. The I/O drive is 12 mA, and you can program the slew rate. The 5000-gate CLi6005, $174.90. **Concurrent Logic Inc,** 1290 Oakmead Pkwy, Sunnyvale, CA 94086. Phone (408) 522-8700. FAX (408) 732-2765. **Circle No. 421**

4-Mbit SRAM module. The PUMA 67S4000 is a 4-Mbit CMOS static-RAM (SRAM) multichip module. The 2.23-in.^{2} surface-mount device comes in a 68-pin ceramic PUMA (pin-uncommitted-memory-array) package. The PUMA package lets you configure the SRAM as 8, 16, or 32 bits wide. The SRAM comes in 25-, 35-, 45-, 55-, or 70-nsec access times. The package is hermetically sealed to conform with MIL-STD-883 specification. Depending on speed, from $610 to $1200 (100). Delivery, 16 weeks ARO. **Mosaic Semiconductor Inc,** 7420 Carroll Rd, San Diego, CA 92121. Phone (619) 271-4565. FAX (619) 271-6058. **Circle No. 422**



TTL-to-ECL translators. The PRL-420N and PRL-420P laboratory tools translate TTL to ECL voltage levels. The PRL-420N has a pair of differential outputs that drive 50Ω loads terminated to −2V. The PRL-420P outputs drive 50Ω loads terminated to 3V. The translators come in a 1 × 1.3 × 2.2-in. aluminum enclosure and operate from a 12 or −12V supply. $90. **Pulse Research Lab,** 1536 W 25th St, San Pedro, CA 90732. Phone (310) 514-1478. FAX (310) 514-0115. **Circle No. 423**

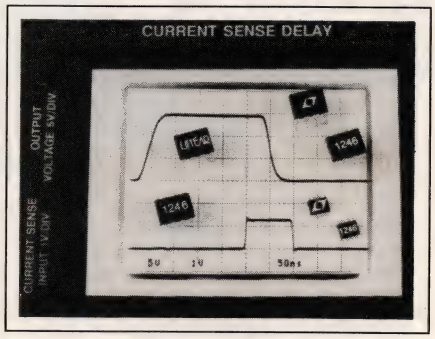
Flash memories. The Am28F010A and the Am28F020A are 1- and 2-Mbit flash memories, respectively. The 12V devices guarantee a minimum of 100,000 endurance cycles. Embedded Program and Embedded Erase algorithms let you automatically program and erase the chips to reduce host-CPU overhead. Am28F010A, $9.90; Am28F020A, $20.75 (100). **Advanced Micro Devices** 901 Thompson Pl, Sunnyvale, CA 94088. Phone (800) 222-9323; (408) 749-5703. **Circle No. 424**

Low-voltage 256-kbit SRAM. The μPD43256B is a 256-kbit static RAM that operates from 2.7 to 5.5V. The chip has a 120-nsec access time when it operates from 2.7V source, and an 85-nsec access time when it operates from 4.5V source. The chip consumes less than 25 μA in standby mode when operating from 3.3V. In power-down mode, the consumption drops to 2 μA. Memory organization is 32k × 8 bits. $5.85 (10,000). **NEC Electronics Inc,** 401 Ellis St, Mountain View, CA 94039. Phone (415) 960-6000. **Circle No. 425**

Servo chip set. This 2-chip set implements a hybrid servo for disk drives having capacities greater than 1 Gbyte. The chip set employs both an embedded and a dedicated servo method to store servo tracking data. The chip set comprises the ML4535 hybrid servo demodulator chip and the ML2377 DSP analog I/O peripheral chip. ML4535, $9.95; ML2377, $6.55 (1000). **Micro Linear Corp,** 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 433-5200. **Circle No. 426**

1-Mbit nonvolatile SRAM. The M48Z128 integrates a 128k × 8-bit CMOS static RAM (SRAM), a power-fail control circuit, and a lithium battery into a 32-pin DIP package. The power-fail circuit monitors the supply line to switch automatically to a battery backup when the supply voltage is out of tolerance. Access time is 85 or 120 nsec. 85-nsec version, $54.60 (1000). **SGS-Thompson,** 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. FAX (602) 867-6102. **Circle No. 427**

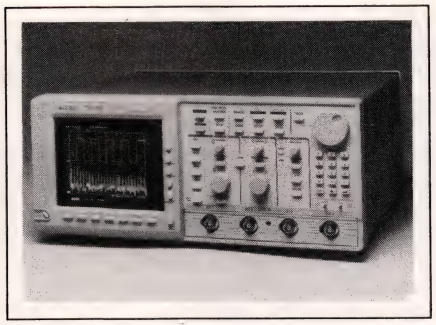
Pulse width modulator. The LT1246 current-mode pulse-width modulator suits off-line switching power supplies. The chip contains a temperature-compensated reference, a high-gain error



amplifier, a current-sensing comparator, and a totem-pole output stage that can deliver 1A. The current delay is 30 nsec, and the chip operates as fast as 1 MHz because there are no cross-conduction current spikes. $2.25 (100). **Linear Technology Corp,** 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (800) 637-5545; (408) 432-1900, ext 365. **Circle No. 428**

3-channel, 6-trace 60-MHz analog scope. The 8060 has a maximum sensitivity of 1 mV/div. On the 1- and 2-mV/div ranges, its bandwidth is 20 MHz. Two channels include delay lines that permit viewing of pretrigger signals. Calibrated delayed sweep allows observing details of long waveforms. $1345. **Leader Instruments Corp,** 380 Oser Ave, Hauppauge, NY 11788. Phone (800) 645-5104; (516) 231-6900.

Circle No. 401



Real-time FFT option for digital scopes. The advanced-math option lets the vendor's TDS 600-series digital scopes perform FFTs with a choice of four windowing functions at rates to 20 transforms per sec. You can use cursors to obtain numeric values of displayed results in logarithmic or linear units and in degrees or radians. $1495 when ordered with a scope; $1995 when added to an existing scope (requires upgrade to V2.0 of the firmware). Delivery, six weeks ARO. **Tektronix Inc,** Box 1520, Pittsfield, MA 01202. Phone (800) 426-2200. **Circle No. 402**

Floppy-disk storage unit for digital scopes. The DSU112, available in 3½- and 5¼-in. versions, works with the vendor's 1600- and 4070/80 series DSOs. The unit stores and replays waveforms and scope setups and allows transferring data to MS-DOS PCs. The 4×6×10-in. unit, which includes an IEEE-488 port, labels all files with sequence numbers and includes an LCD and keypad that lets you select specific files. $1795. **Gould Inc,** 8333 Rockside Rd, Valley View, OH 44125. Phone (216) 328-7000. FAX (216) 328-7400.

Circle No. 403

$994 data-acquisition hardware/software package for MS-DOS PCs. A package consisting of the vendor's DAS-1600 board and Easyest AG software acquires data from as many as 160 channels (10 boards). The software converts signals from B, E, J, K, R, S, and T thermocouples into engineering units. It also produces a "strip-chart" display and allows optimization of control systems that use the proportional-integral-derivative (PID) algorithm. **Keithley Metrabyte,** 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. FAX (508) 880-0179. **Circle No. 404**

Distributed I/O package for factory automation. The combination of the Workhorse I/O system and Intellution Inc's Fix DMACS software allows data acquisition, process control, and data management in hostile factory environments. The hardware and software, which are compatible with computers running under MS-DOS, MS-Windows, and OS/2, are modular and configurable so that you can adapt them to evolving needs. $11,000 to $13,000. **Keithley Metrabyte,** 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. FAX (508) 880-0179. **Circle No. 405**

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CIRCLE NO. 70

NEC

Potentiometer. The Durapot wiperless potentiometer offers a 4- to 20-mA, 3-wire output as well as outputs of 0 to 10V or −10 to +10V. It reads shaft position with 0.05% accuracy, has no mechanical stops, and is available in versions which have 1, 5, or 10 turns. The internal sensing element is a stainless-steel resolver. The devices are packaged in NEMA 12, 13, 4X, or corrosion-resistant housings to withstand heavy-duty, hostile environments. From $100. **Astrosystems Inc,** 6 Nevada Dr, Lake Success, NY 11042. Phone (516) 328-1600. TWX 510-223-0411. **Circle No. 406**

Sealed keyboard. This 42-position sealed keyboard is designed for harsh industrial environments. It features a polyester front sheet bonded onto a steel plate to provide NEMA 4 or 4X sealing. The unit can operate with IBM PC/AT- and PS/2-based control systems; an optional RS-232C interface provides compatibility with a wide range of DEC computers. $447. **Computer Keyboard Systems Ltd,** 1640 Fifth St, Suite 224, Santa Monica, CA 90401. Phone (310) 395-4639. FAX (310) 393-6040. **Circle No. 407**

RF connectors. This line of RF connectors includes BNC, TNC, Twinax, UHF, Mini-UHF, F-Style, and between-series-adapter (BSA) devices. The mounting styles include bulkhead, panel, and pc-board designs. The termination versions are crimp-crimp, clamp-solder, and screw-on. Plating options include nickel, silver, gold, and black chromate. $1.86 (5000) for a BNC T-adapter with a nickel body and silver contacts. **Molex Inc,** 2222 Wellington Ct, Lisle, IL 60532. Phone (708) 969-4550. FAX (708) 969-1352. **Circle No. 408**

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Supply Sensitivity — 0.2%/V	T_{PD} — 1.5 ns
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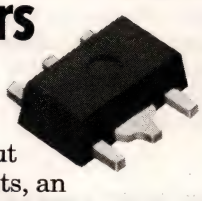

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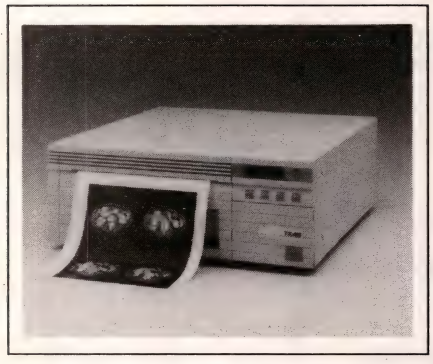


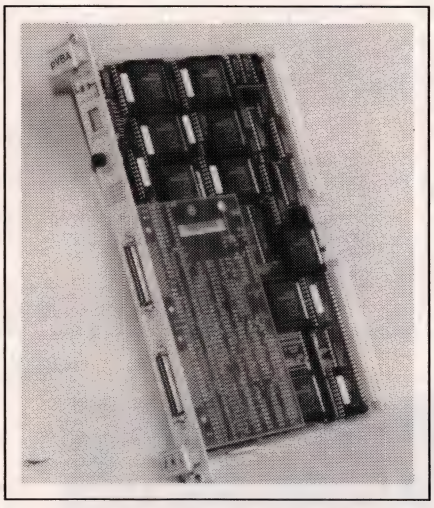
Video printer. The TP-6530 video printer gives 256 levels of gray and 300-dpi resolution on black-and-white dye sublimation paper. Its maximum dot-clock frequency of 135 MHz makes it compatible with standard workstations. The unit tunes automatically to NTSC, PAL, (phase-alteration line), or 1280×1024 workstation video formats. Maximum hard-copy size is 6.5×8.5 in. $7975. **Team Systems Inc,** 2934 Corvin Dr, Santa Clara, CA 95051. Phone (800) 338-1981; (408) 720-8877. FAX (408) 720-9643. **Circle No. 409**

Small, hazardous-location workstation. The Series 110/120 PLC workstation has UL approval and CSA certification for installation in Class I, Div 2 and Class II, Div 2 hazardous locations for Groups A, B, C, D, F, and G. The 10.5×6×4-in. unit connects to programmable controller serial ports to provide alternatives to keypads, thumbwheels, message displays, annunciator panels, pushbuttons, and indicator lights. From $995. **Nematron Corp,** 5840 Interface Dr, Ann Arbor, MI 48103. Phone (313) 994-0501. FAX (313) 994-8074. **Circle No. 410**

SPARCstation upgrade. The MBus engine/System-III runs at 28.5 SPECmarks and 32 MIPS. It has onboard color graphics and two SBus expansion slots. The board runs the Solaris operating system and all SPARCware applications. Less than $8000. **Pinnacle Data Systems Inc,** 1350 W Fifth Ave, Columbus, OH 43212. Phone (614) 487-1150. **Circle No. 411**

Encryption unit. The Datacryptor 64E secures communications in public and private X.25 packet-switched networks. It encrypts data at speeds as high as 64 kbps in either the Data Encryption Standard (DES) or a proprietary algorithm. The unit complies with ANSI's Key Management Standard and the National Institute of Standards and Technology's (NIST) FIPS 140 for use in government and commercial applications. It will be available in January 1993. $2900. **Racal-Datacom Inc,** Box 407044, Fort Lauderdale, FL 33340. Phone (305) 846-1601. FAX (305) 846-3935. **Circle No. 412**

VME/VSB bus adapter for VAXstations. The pVBA module is a 6U-format Eurocard that combines fast VME/VSB bus interfaces and a cabled connection



to a host adapter card in a VAXstation. It offers VAX users access to a large base of VME real-time products. The pVBA controls and communicates with VME slave and master modules and can serve as a system controller. Upgrade for existing workstations, $3995; full system with VME chassis, from $9500. **Zeller Research Ltd,** 500 Wood St, Bristol, RI 02809. Phone (401) 254-0270. FAX (401) 254-0294. **Circle No. 413**

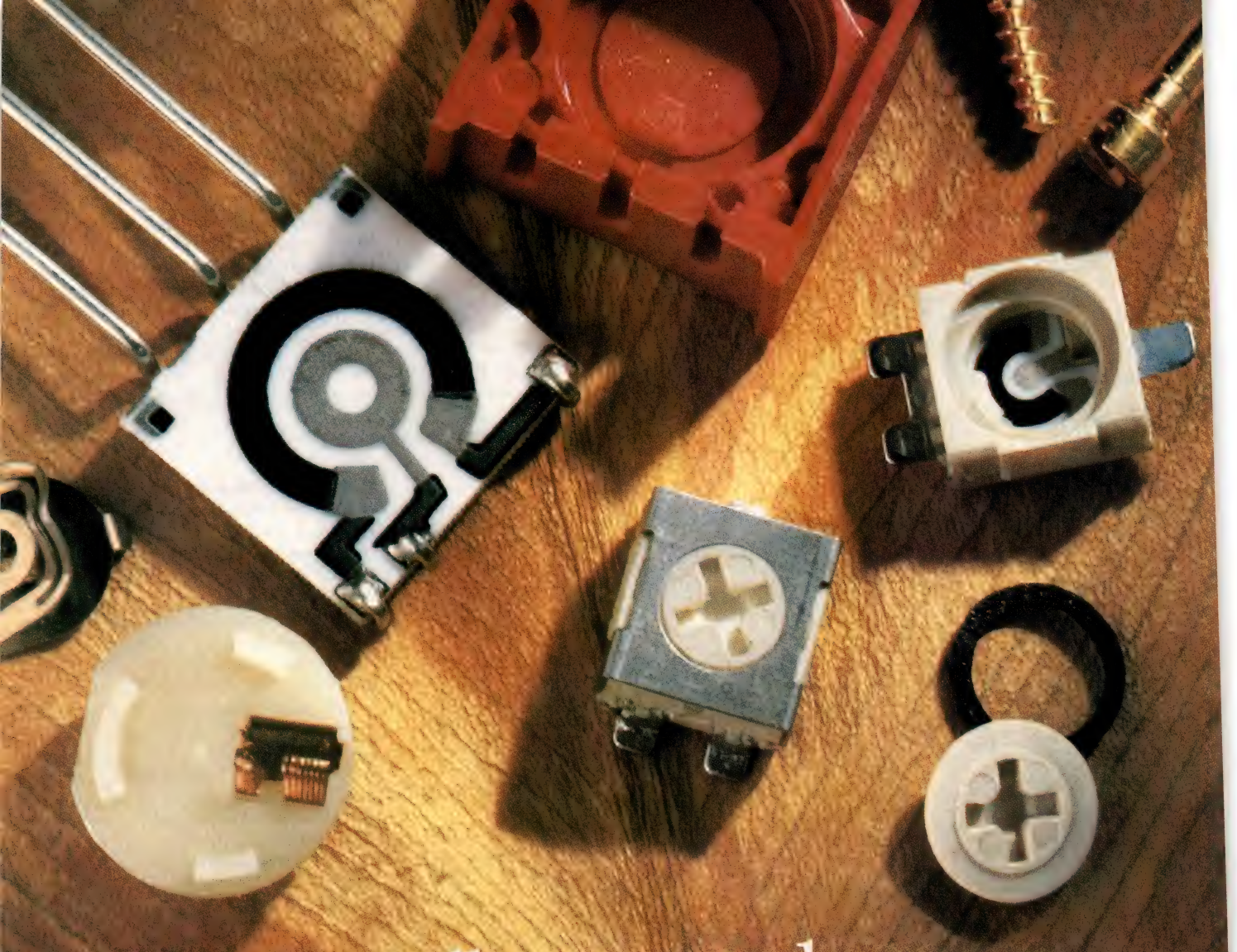
Color-LCD controller for VME. The VCD-V VMEbus graphics controller drives the Sharp LQ9D011 8.4-in. multicolor TFT-LCD flat-panel display and other flat-panel and CRT displays. It uses the TMS34020 graphics processor and has both analog and digital output ports. From $1800. **Peritek Corp,** 5550 Redwood Rd, Oakland, CA 94619. Phone (510) 531-6500. FAX (510) 530-8563. **Circle No. 414**

VME breadboard. The Protokit is a VMEbus interface kit for designing custom I/O and memory boards. It includes a mezzanine prototype board and a 68030-based CPU board. The two units connect via the SAMbus, a local 32-bit expansion bus. The prototype board's space divides in two, allowing use of memory mezzanines. $1295. **General Micro Systems,** 8358 Maple Pl, Rancho Cucamonga, CA 91730. Phone and FAX (714) 980-4863. **Circle No. 415**

VME-to-PC expansion products. The XVME-956 line of expansion products allows integration of PC/XT and PC/AT modules into VMEbus systems. Standard PC/104 modules provide the PC functions; they install on an XVME-956 carrier card. Expansion devices from the manufacturer include a serial/parallel port, a SCSI controller, an Ethernet interface, and a memory-expansion module. $350 to $500. **Xycom Inc,** 750 N Maple Rd, Saline, MI 48176. Phone (800) 367-7300; (313) 429-4971. FAX (313) 429-1010. **Circle No. 416**

Rugged VGA display. The EL-VGATP unit is a rugged, compact high-resolution flat-panel display suitable for use in exposed environments of high shock and vibration. The display is sealed to NEMA 4/12 standards and provides a 100:1 contrast ratio and a viewing angle of more than 160°. An infrared touch panel is optional. From $2595. **Kinetic Computer Corp,** 82 Grandview Rd, Arlington, MA 02174. Phone (617) 547-2424. FAX (617) 547-7266. **Circle No. 417**

Stereo mixer for PC multimedia. The MX-33 stereo mixer provides 3-input balancing and mixing of audio from CD-ROM, a PC, or video disk. It supplies a composite signal for a fixed-level, preamplifier or amplifier output or an adjustable dual-headphone output. Front-panel controls balance input amplitudes. $185. **Antex Electronics,** 16100 S Figueroa St, Gardena, CA 90248. Phone (310) 532-3092. FAX (310) 532-8509. **Circle No. 418**



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Analog-voice-networking software. AMIS (Audio Messaging Interchange Specification) analog-networking software allows the exchange of voice messages between the company's and other voice processing systems. It features time and date stamp, message forwarding, and choice of message delivery: immediate, overnight, or as much as one year in advance. $3000. **VMX Inc,** 2115 O'Nel Dr, San Jose, CA 95131. Phone (408) 441-1166. **Circle No. 430**

68000 series cross tool kit for HP 9000. The 680x0 Cross Tool Kit includes Green Hills C, Fortran, and Pascal cross-compilers for the Oasys 68K Cross Assembler/Linker System. The kit allows you to target applications to the Motorola 68000 series, 683xx, and 68881/882 microprocessors using an HP 9000 Series 700 PA-RISC workstation. From $3600. **Oasys Inc,** 1 Cranberry Hill, Lexington, MA 02173. Phone (617) 862-2002. **Circle No. 431**

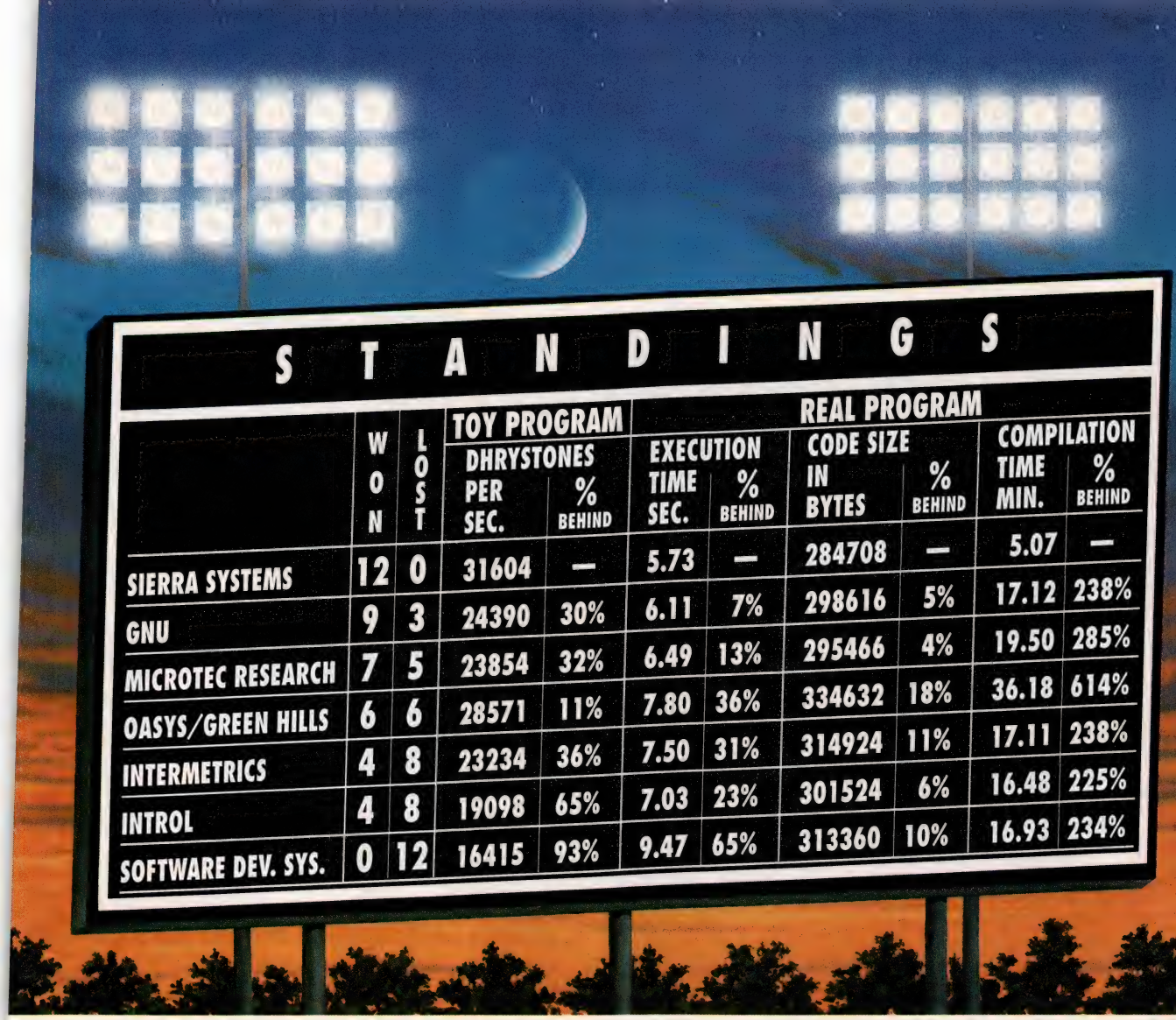
Dial-up modem-management system. Global View 2.0 MS-Windows-based, modem-management system lets a central-site operator manage hundreds of dial-up modems from a single console. This version allows use of synchronous modems with security devices for controlling authorized connections. The system tracks every call and stores that information in compressed files. $5000. **UDS Motorola Inc,** 5000 Bradford Dr, Huntsville, AL 35805. Phone (800) 451-2369; (205) 430-8000. FAX (205) 430-8208. **Circle No. 432**

32-bit, pc-board-layout tools. Ultiboard V4.5 32-bit layout software includes an autorouter, real-time design rule checking on trace manipulation, block import/export and rotate, bidirectional interface with the majority of schematic capture packages, auto junction/snap-to-pin, automatic polygon editing, and immediate reconnect, force vector, and histogram update when you move components. From $595 for DOS version to $9950 for Professional Engineer Unix version. **Ultimate Technology BV,** Box 5166, 1410 AD Naarden, The Netherlands. Phone (31) 2159-44424. FAX (31) 2159-43345. **Circle No. 433**

Analog, mixed-signal and signal-integrity tools. Contec CAE version 2.0 has a common X-Window interface, mathematical and graphical postprocessor functions, and a node-suppression algorithm; these features allow the products to simulate circuits two to three times the size of circuits simulated using Spice3. The simulation device also includes charge- and flux-linkage-based, local-truncation-error calculation; transient step-size control, analysis speed, and analysis-convergence properties; and function continuity in device-modeling equations to ensure convergence. PC licenses, from $4700; Sun workstation licenses, from $9100. **Contec Microelectronics USA Inc,** 2188 Bering Dr, San Jose, CA 95131. Phone (408) 434-6767. FAX (408) 434-6884. **Circle No. 434**

FPGA design kit for Mentor 8.0. The Design Kit allows you to utilize Mentor Graphics Design Architect and Quicksim II tools for schematic capture and simulation of the Crosspoint Solutions' CP20K family of FPGAs. This family has gate-array architecture with transistor-level granularity, which eliminates the design step of "fitting" associated with non-gate-array architectures. Design Kit license, $4950. **Crosspoint Solutions Inc,** 5000 Old Ironsides Dr, Santa Clara, CA 95054. Phone (408) 988-1594. FAX (408) 980-9594. **Circle No. 435**

Disk-mirroring software. Immunity Plus 1.0 provides continuous, real-time backup of the user's data and adds fault-tolerant operations to any PC-compatible computer without adding extra hardware. The software runs invisibly in the background, mirroring every write operation to a secondary hard-disk drive. $249. **Unitrol Data Protection Systems Inc,** Suite 604, 815 Hornby St, Vancouver, BC V6Z 2E6, Canada. Phone (800) 665-2212; (604) 681-3611. **Circle No. 436**



68000 Compiler Benchmark Results.

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Won/Lost Record: For each benchmark, the compilers' run-time performances were compared to each other with wins and losses totalled in round-robin fashion. (See Dhrystones and Execution Time columns on scoreboard.)

Compilers: GNU 2.0, Intermetrics 8.0, Introl 3.06, Microtec Research 4.2d, Oasys/Green Hills 1.8.5Rc, Sierra Systems 3.0, Software Development Systems 5.1.

Hosts: 33 MHz 386 Zeos PC and Sun SPARCstation IPC. All compilers were run on the PC, except for GNU and Oasys/Green Hills, which were run on the Sun. Running the Sierra Systems compiler on both host systems allowed the Sun times to be scaled to PC time for the scoreboard.

Target: Motorola VME167, 25 MHz 68040 with caches enabled.

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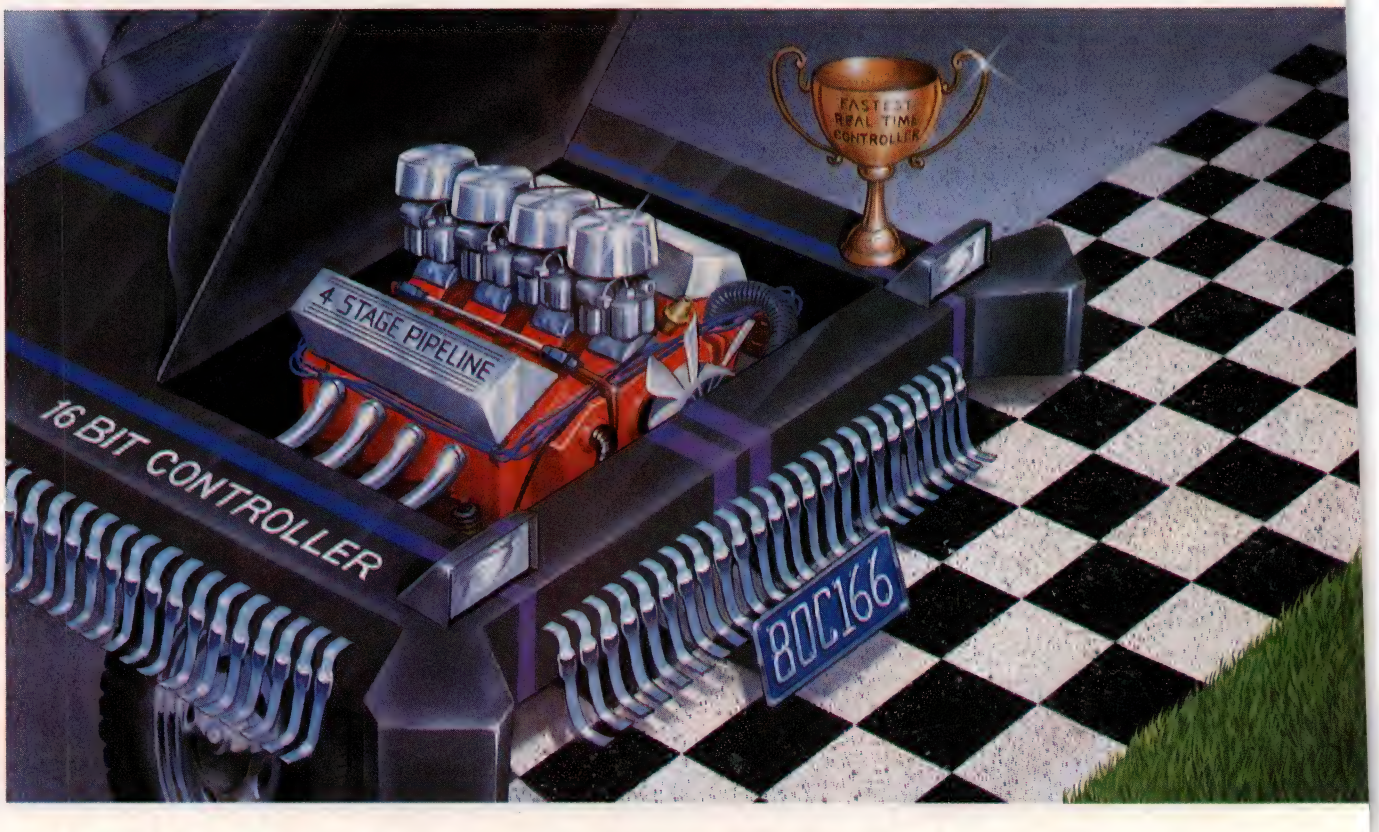

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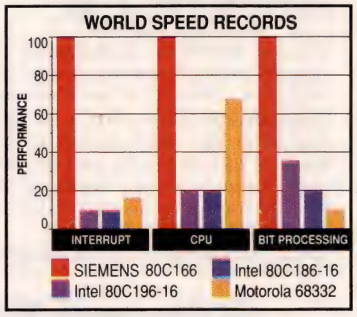

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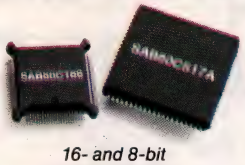

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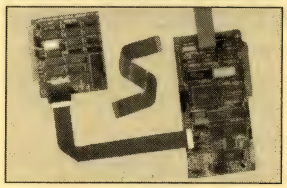

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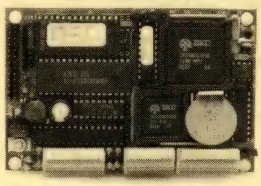

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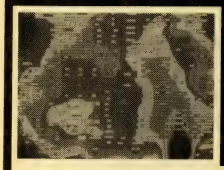

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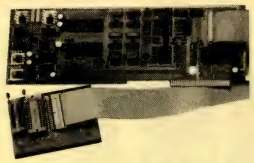

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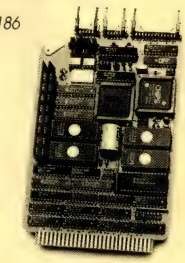

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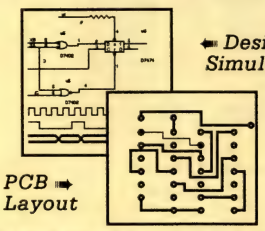

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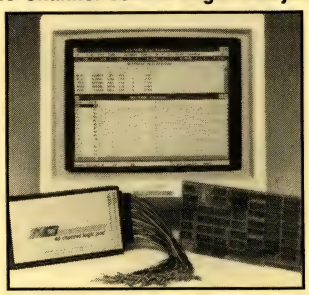

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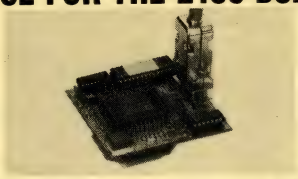

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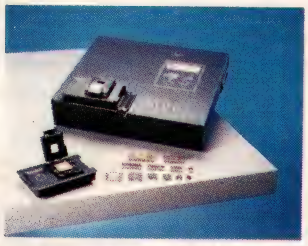

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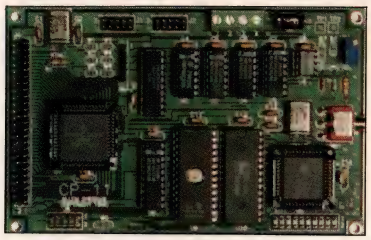

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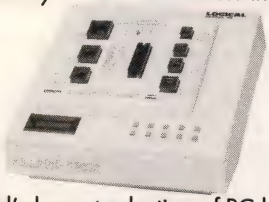

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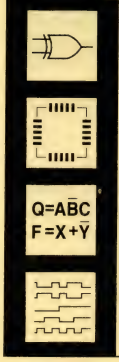

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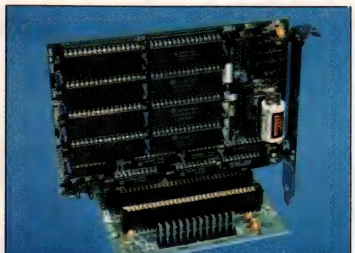

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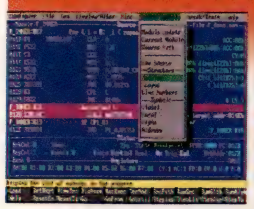

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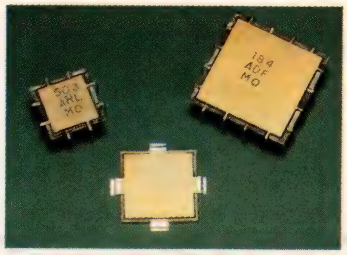

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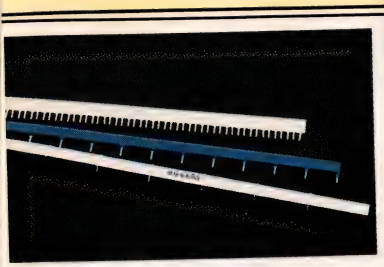

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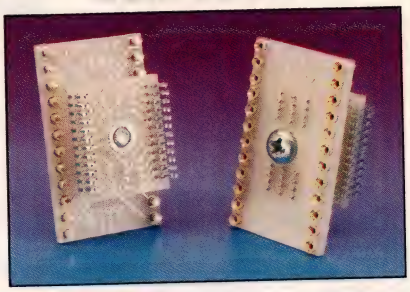

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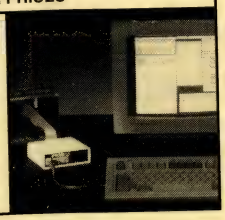

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EDN Products & Careers	Jan. 14	Dec. 29	Buyers Guide: Communications • Product Focus: Hardware & Interconnect • Product Preference Survey • Career Opportunity: Computer Peripherals • Diversity Series
EDN Magazine	Jan. 21	Dec. 30	DSP/Image Compression—Part I • Designing ASICs—Part II • PLDs • Technical Article Database Index
EDN Products & Careers	Jan. 28	Jan. 13	Buyers Guide: Memory Technology • Product Focus: Disk Drives • Hot Products: Buscon West • Career Opportunity: Medical Electronics (Includes software) • Regional Profile: N. Carolina, S. Carolina, Georgia
EDN Magazine	Feb. 4	Jan. 15	Software Development • Designing ASICs—Part III • Power Sources • FPGAs
EDN Products & Careers	Feb. 11	Jan. 27	STATE OF ENGINEERING SUPPLEMENT • Annual Salary Survey • Buyers Guide: Test & Measurement • Product Focus: Digital ICs • Product Preference Survey • Career Opportunity: Telecommunications (Includes software)
EDN Magazine	Feb. 18	Jan. 29	Memory Technology • Graphics Technology Computer Buses • Analog ICs • Designing ASICs—Part IV
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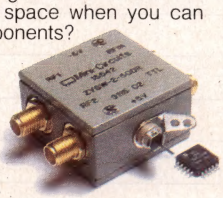

SPECIFICATIONS (typ)	Absorptive SPDT YSWA-2-50DR ZYSWA-2-50DR			Reflective SPDT YSW-2-50DR ZYSW-2-50DR		
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Ins. Loss (dB)	1.1	1.4	1.9	0.9	1.3	1.4
Isolation (dB)	42	31	20	50	40	28
1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	——	20	——	22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
Video Bkthru (mV,p/p)	30	30	30	30	30	30
Sw. Spd. (nsec)	3	3	3	3	3	3
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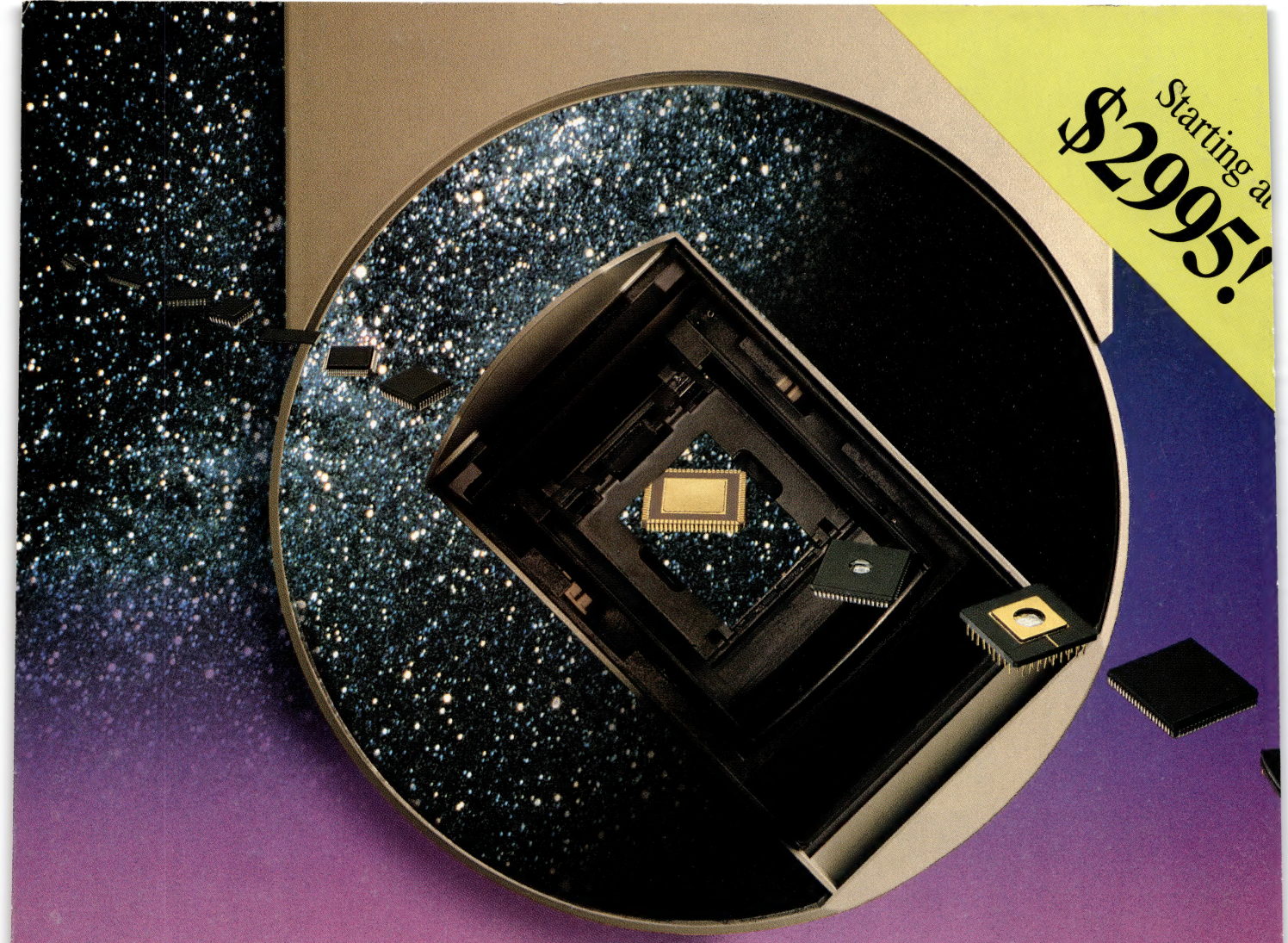

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